

Redwood 11.6" Schematic Document

Bay Trail - M

2014-04-01

REV : A00

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DY : None Installed

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Title

Cover Page

Size
A3

Document Number

Redwood 11.6"

Rev

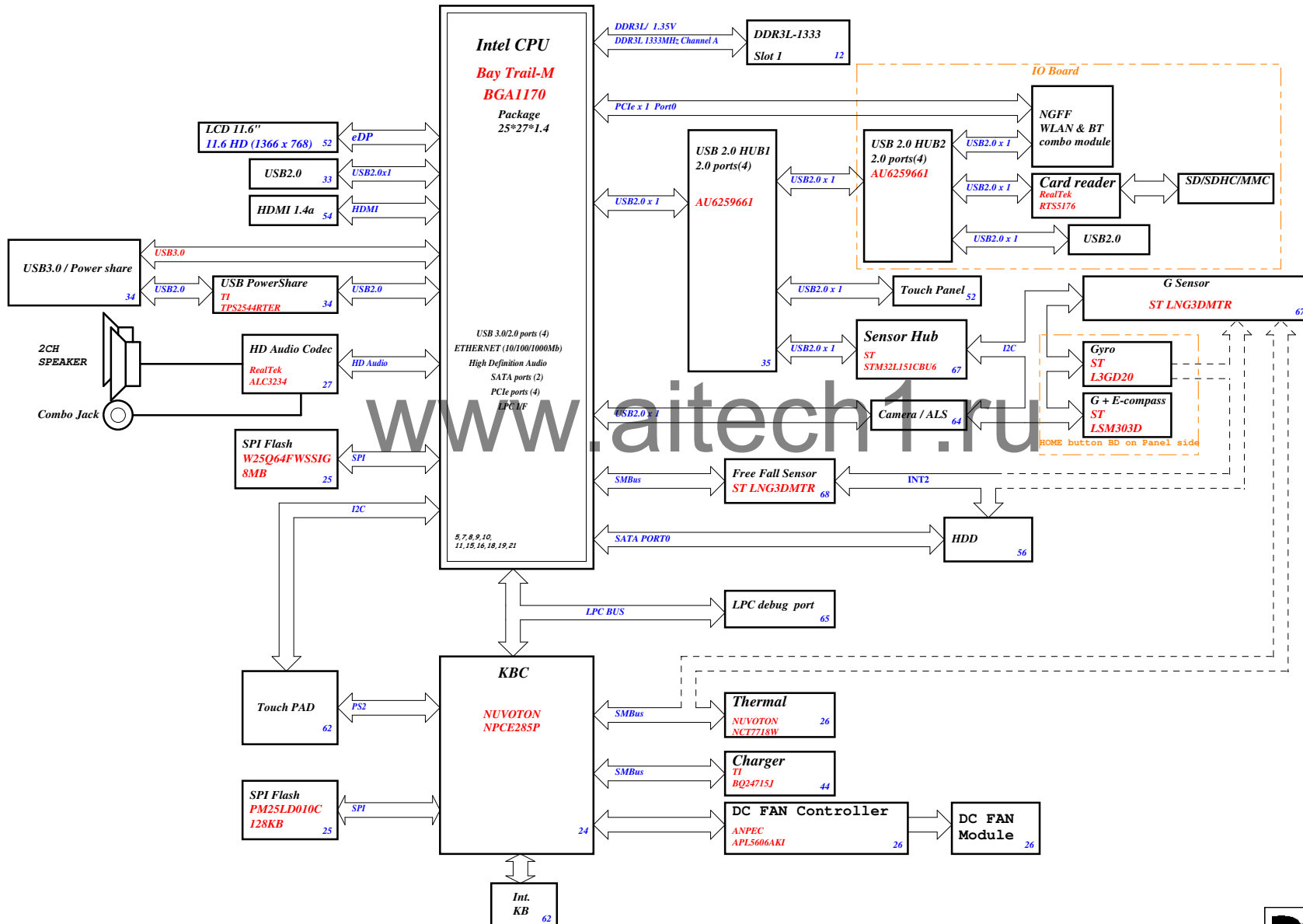
A00

Date: Tuesday, April 01, 2014

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Redwood 11.6" Board Block Diagram

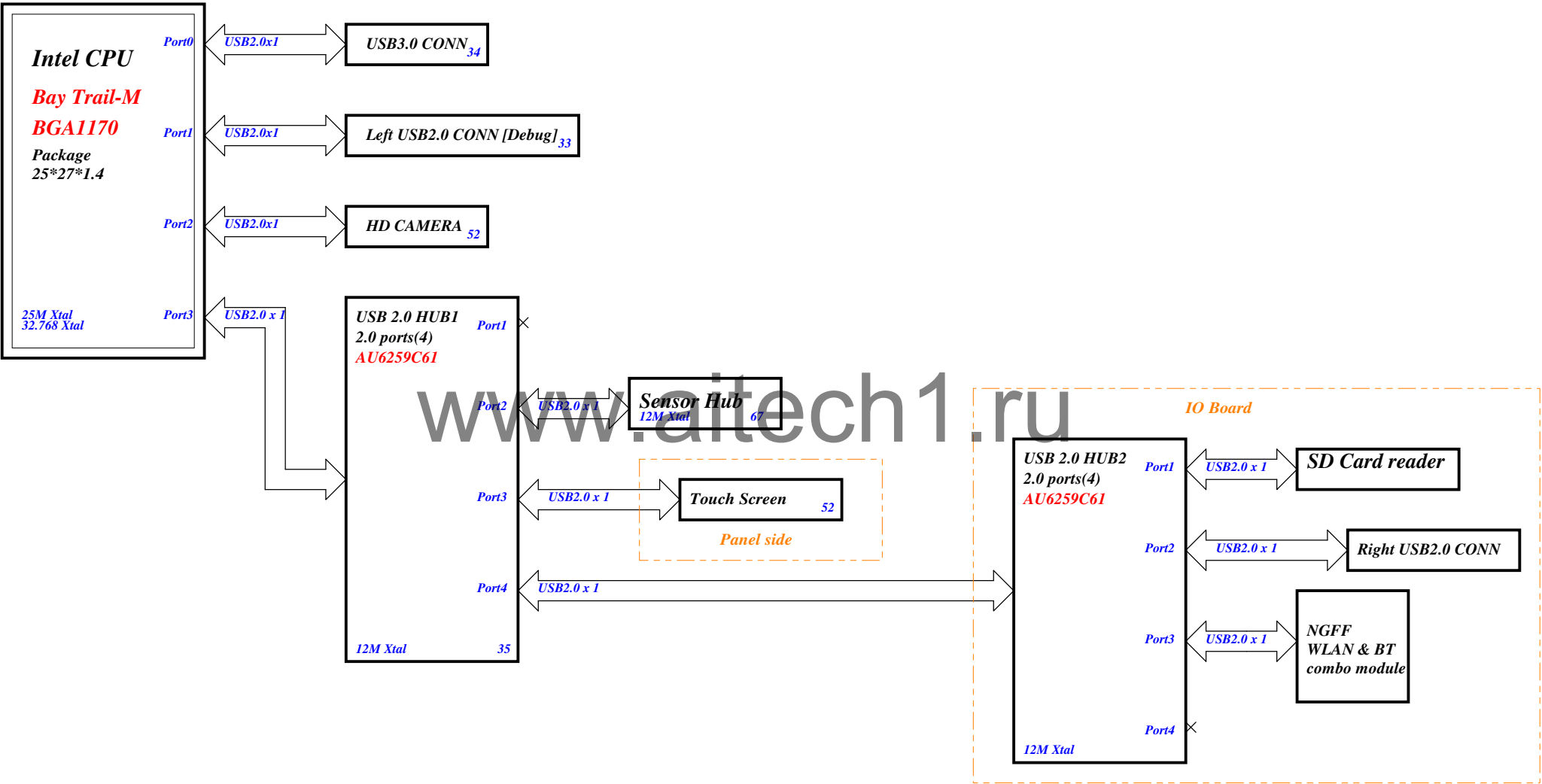
Project code : 4PD00K010001
PCB P/N : 13270
Revision : -1



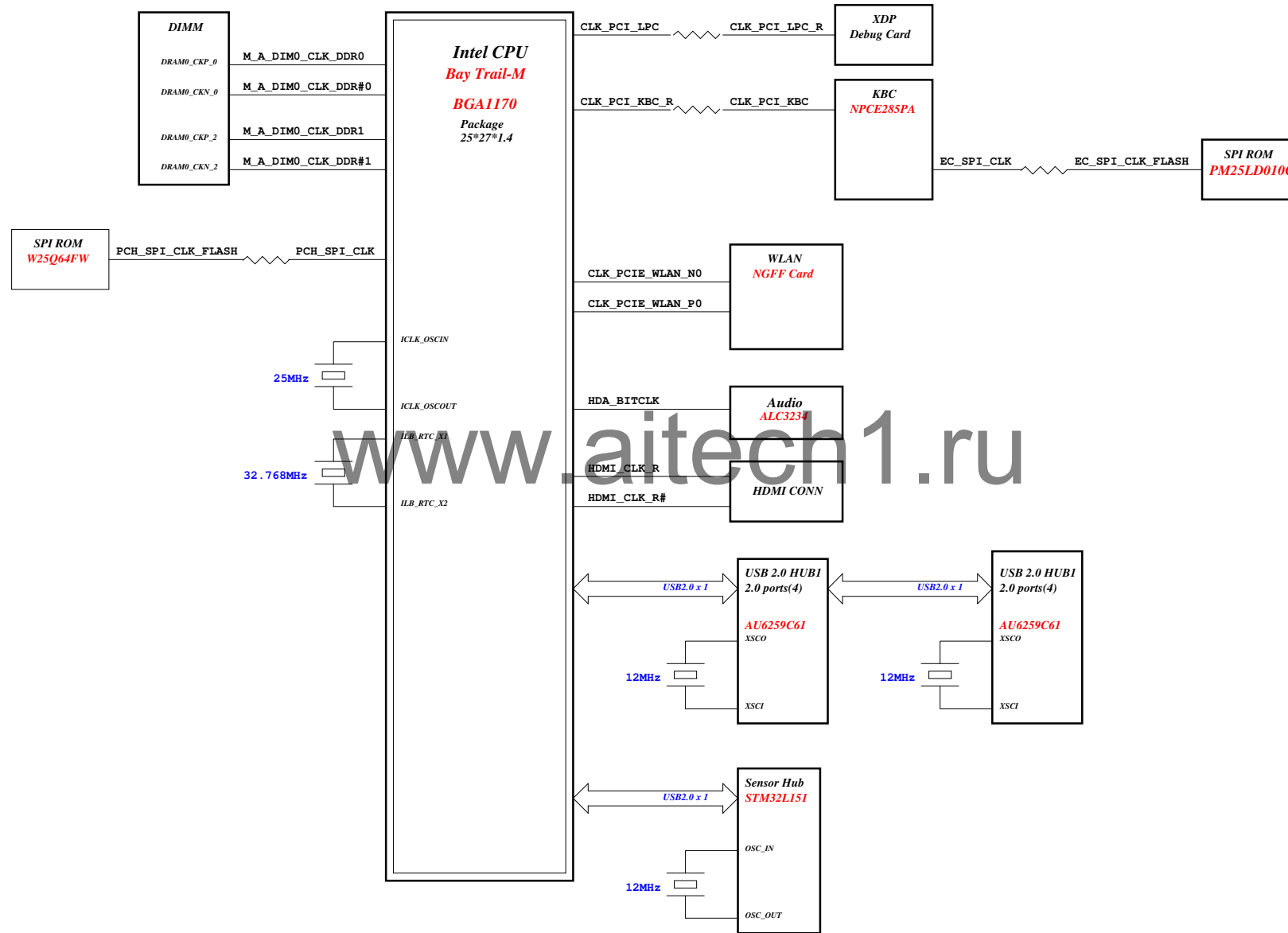
CHARGER	BQ24715J	44
INPUTS	OUTPUTS	
DCBATOUT	BT+	
SYSTEM DC/DC	TPS51225	45
INPUTS	OUTPUTS	
DCBATOUT	5V_S5	
	3d3V_S5	
CPU DC/DC	ISL95833	46-47
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
SYSTEM DC/DC	SY8206	50
INPUTS	OUTPUTS	
DCBATOUT	1d0V_S5	
SYSTEM DC/DC	TPS51363	49
INPUTS	OUTPUTS	
DCBATOUT	1d35V_S3	
SYSTEM LDO	TLV70218	51
INPUTS	OUTPUTS	
	3d3V_S5	1d8V_S5
SYSTEM LDO	TLV70215	51
INPUTS	OUTPUTS	
	3d3V_S5	1d5V_S0
Step Down Regulator	SYW232	51
INPUTS	OUTPUTS	
	1d0V_S0_P6	1d05V_S0
LOAD SWITCH	TPS22966	37
INPUTS	OUTPUTS	
	1d8V_S5	1d8V_S0
LOAD SWITCH	TPS22965	37
INPUTS	OUTPUTS	
	1d0V_S5	1d0V_S0

PCB LAYER
L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

USB Port Block Diagram



Clock Block Diagram




SSID = CPU

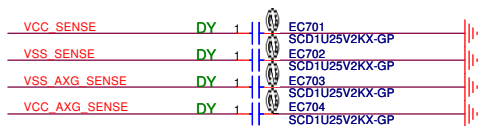
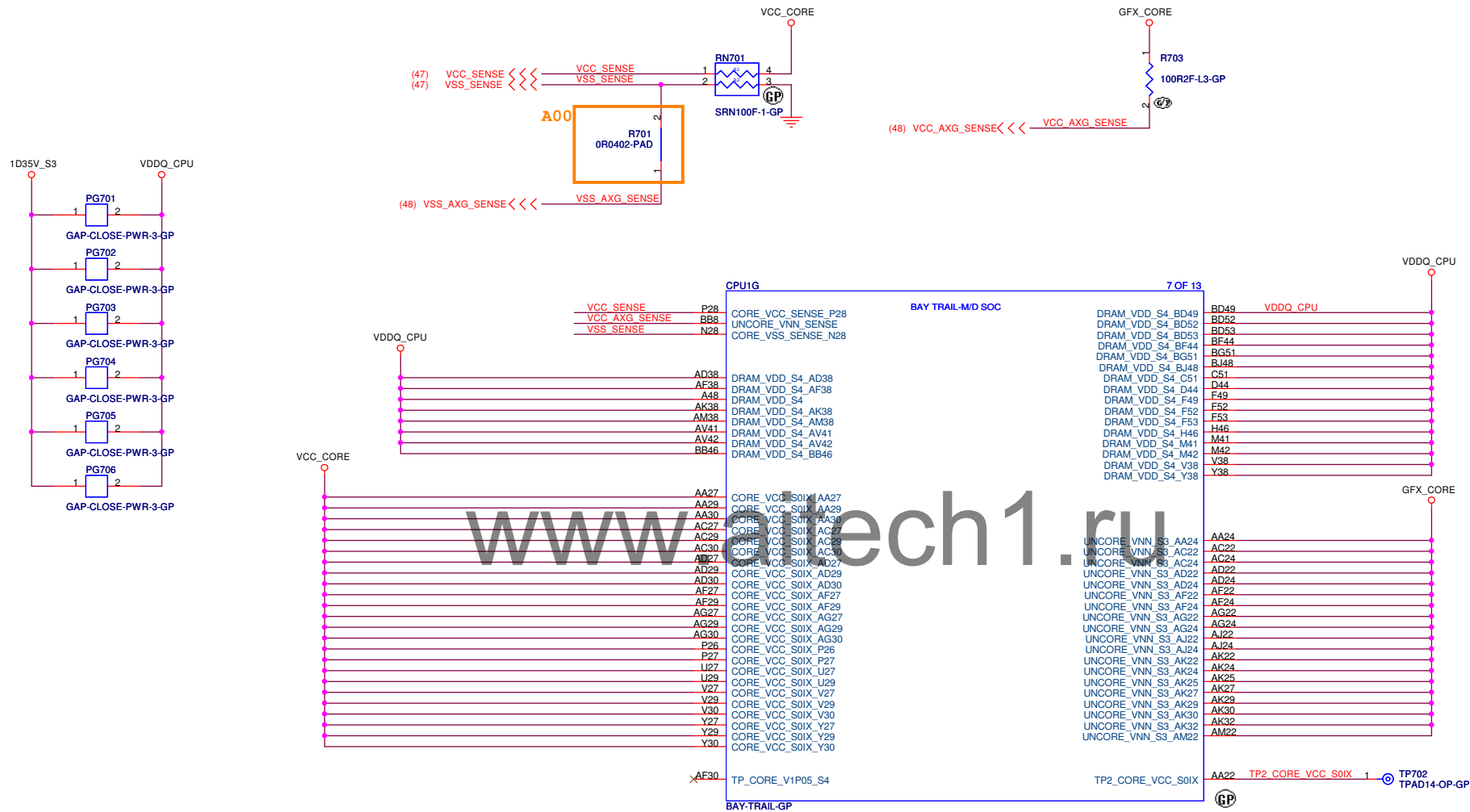
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Title CPU (CFG)		
Size A4	Document Number Redwood 11.6"	Rev A00
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SSID = CPU



reserve the 0402 0.1u caps on reset for EMI.

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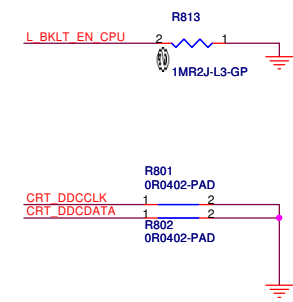
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Title			CPU (VCC CORE)		
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SSID = CPU



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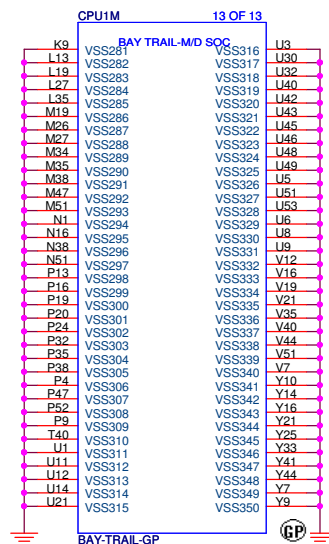
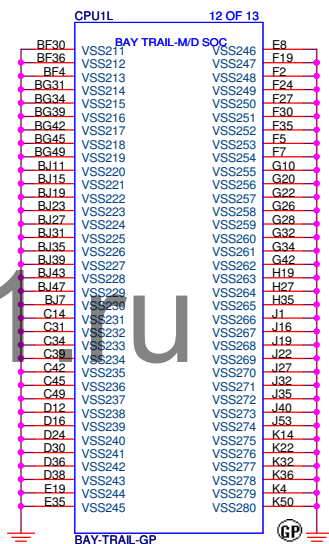
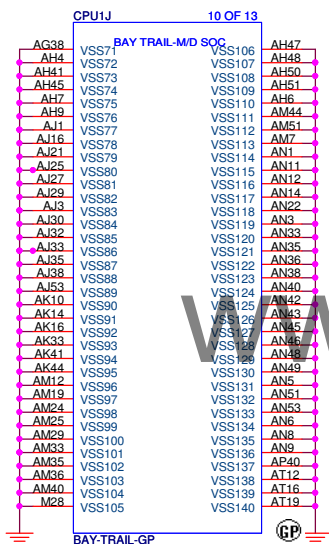
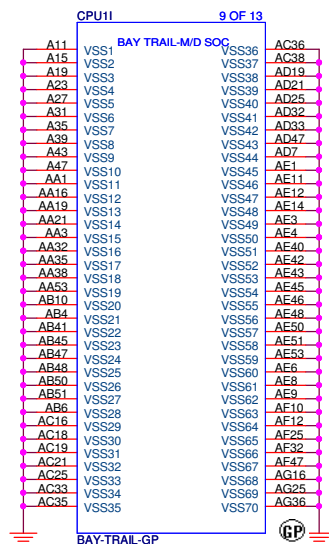
**CPU (DDI/EDP/GPIO)**

Rev

Redwood 11.6"

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SSID = CPU



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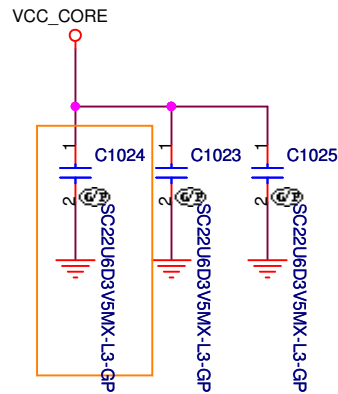
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Title: **CPU (VSS)**

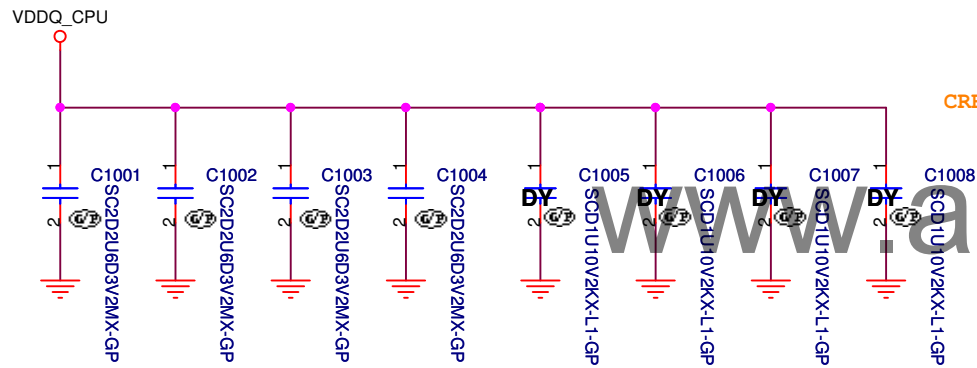
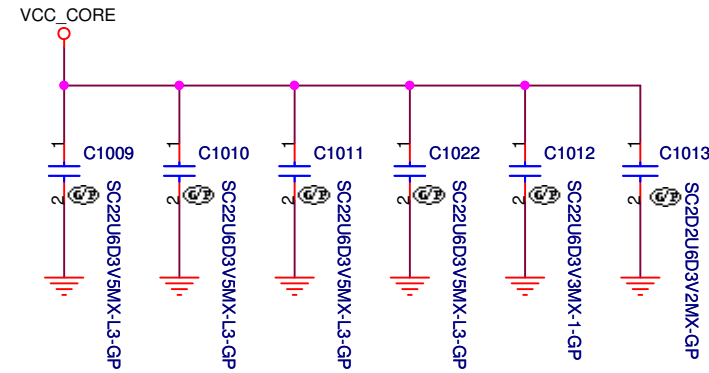
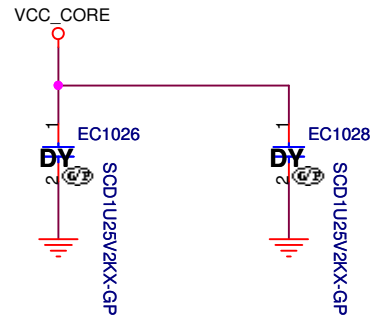
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reserve the 0402 0.1u caps on reset for EMI.

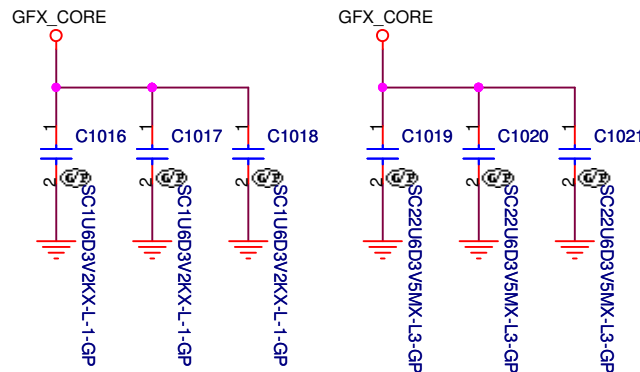
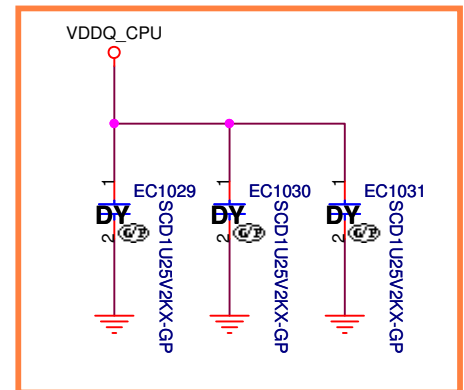
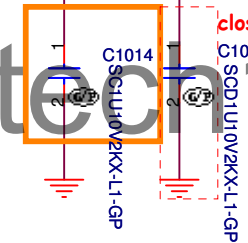


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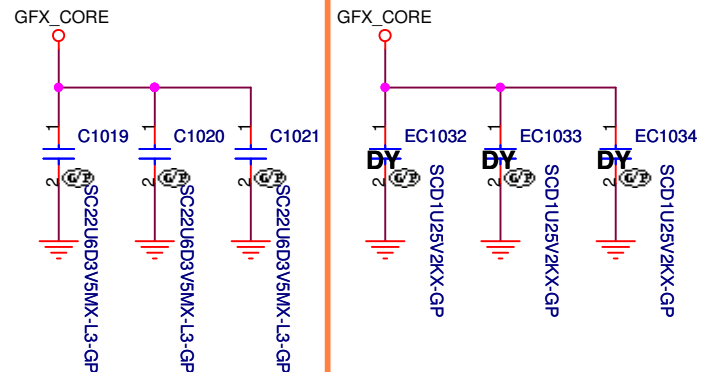


CRB放1uF

close to pin AD38 & AF38



reserve the 0402 0.1u caps on reset for EMI.



reserve the 0402 0.1u caps on reset for EMI.

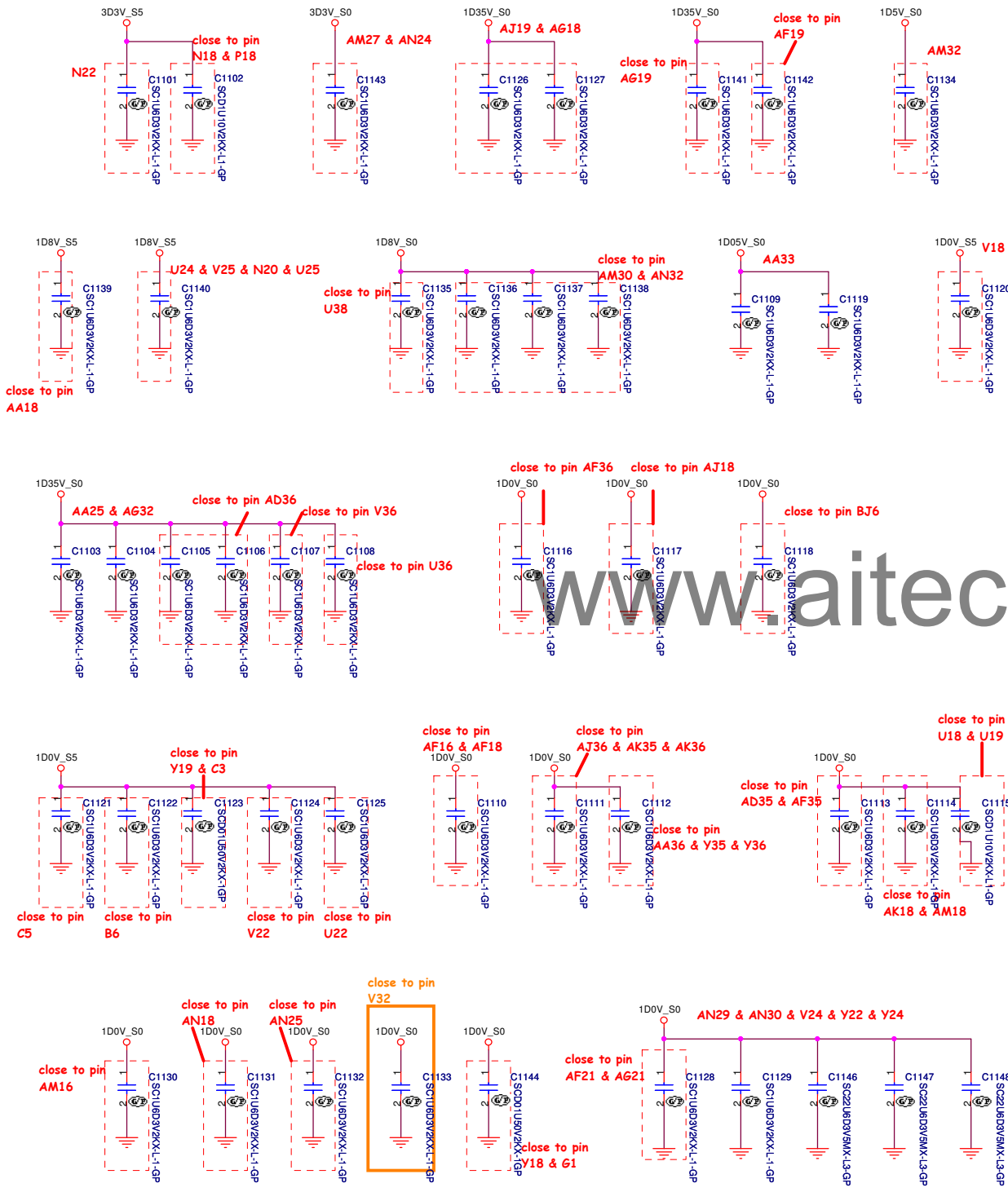
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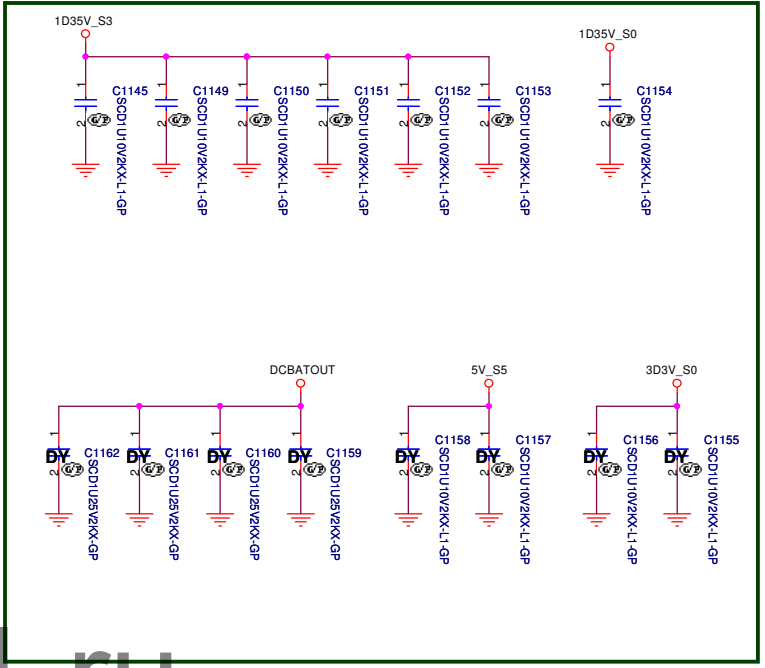


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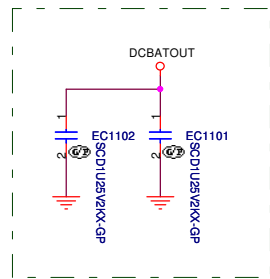
Title CPU (Power CAP1)		
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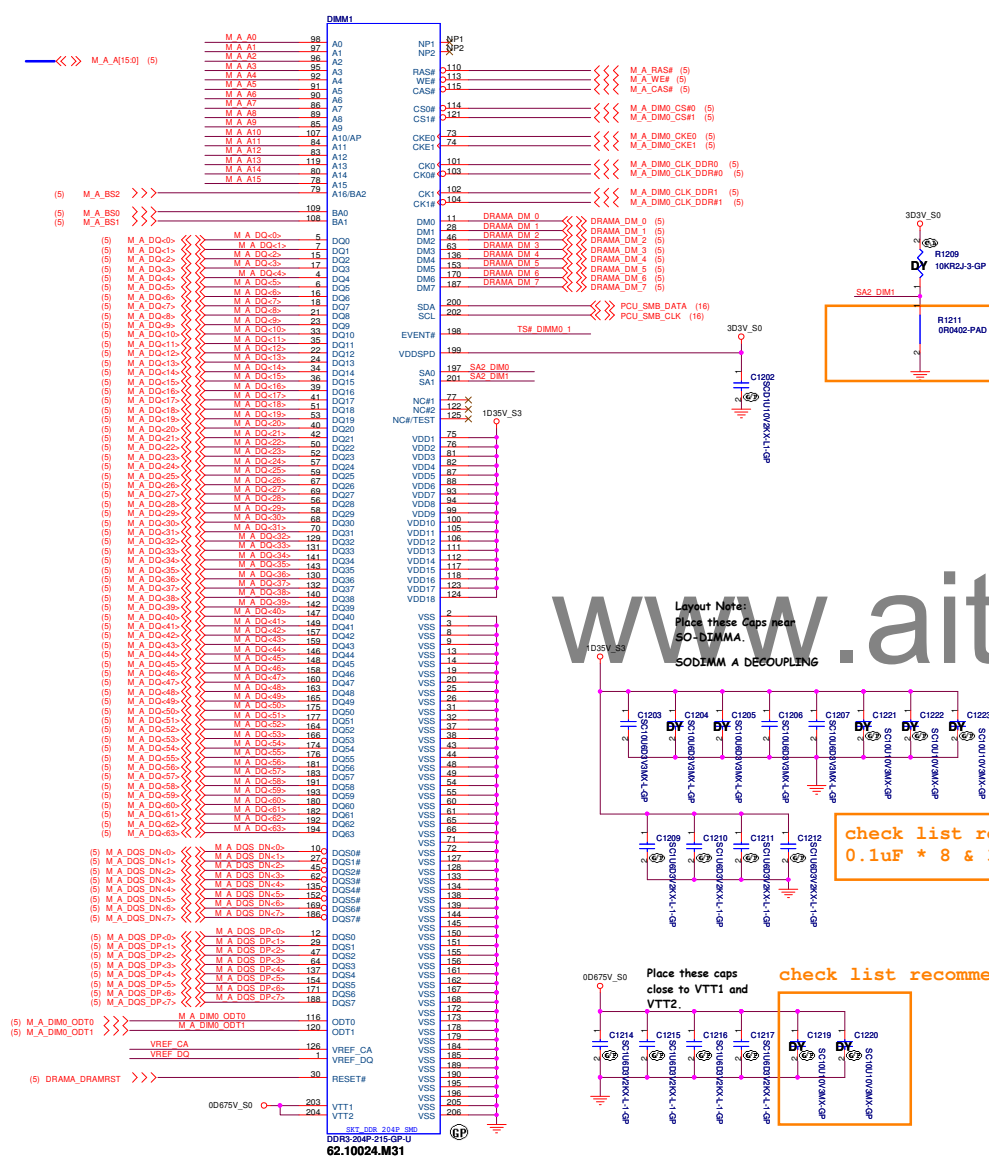


X02 RF requirement



X02 EMI requirement





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SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

EDS_Revlp5 define the strap removed for MDSI P.21

Description	BIOS Boot Selection	Security Flash Descriptors	DDI0 Detect	DDI1 Detect	DDI1 Detect	Top swap
GPIO	GPIO_S0_SC[063]	GPIO_S0_SC[065]	DDI0_DDCDATA	DDI1_DDCDATA	MDSI_DDCDATA	GPIO_S0_SC [56]
Schematic						
High	SPI	Normal Operation	DDI0 detected	DDI1 detected	DDI1 detected	
Low	LPC	Override	DDI0 not detected	DDI1 not detected	DDI1 not detected	

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2.25 Hardware Straps

All straps are sampled on the rising edge of PMC_CORE_PWROK.

30.2 LPE_I2S2_DATAOUT/ GPIO_S0_SC[065]ball as Flash Descriptor Security Override

In order to update the entire flash during manufacturing process or as part of a board return flow, the flash Descriptor Security override ball BC30 (GPIO_S0_SC[065]) can be used to unlock the entire SPI flash (override descriptor setting) and to stop the Intel® TXE from accessing SPI.

For full description and implementation data, please refer to the Bay Trail M/D "Manufacturing Recommendations" document, CDI #515108, section #2.6.

27.1.1.2 Hardware Controlled

System hardware, external to the SoC, can be used to assert or de-assert the Top-Swap strapping input signal. If the signal is sampled as being asserted during power-up then Top-Swap is active.

Note: The Top-Swap strap is an active high signal and is multiplexed with the GPIO_S0_SC[56] signal.

Table 27. Straps

Signal Name	Function	Default	Strap Exit	Strap Description
GPIO_S0_SC[63]	Legacy	1b	PMC_CORE_PWROK de-asserted	BIOS Boot Selection 0 = LPC 1 = SPI
GPIO_S0_SC[65]	Legacy	1b	PMC_CORE_PWROK de-asserted	Security Flash Descriptors 0 = Override 1 = Normal Operation
DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected
MDSI_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

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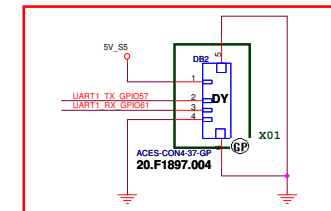
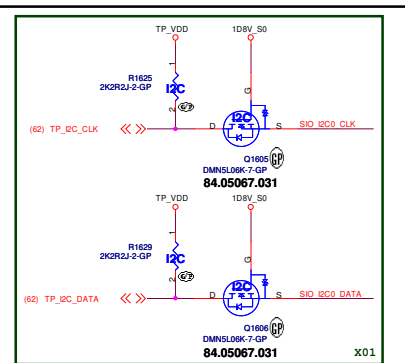
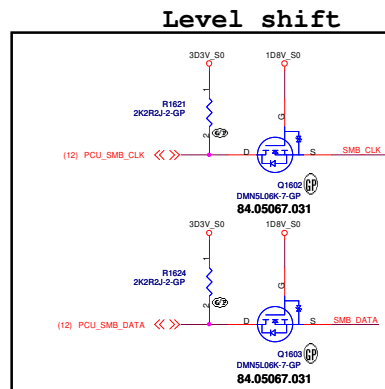
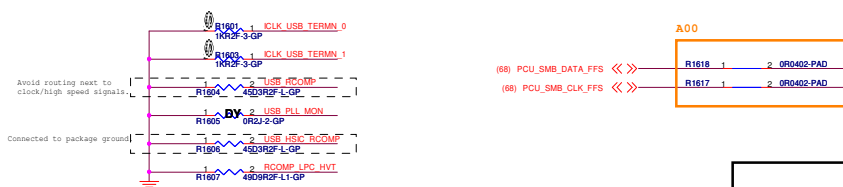
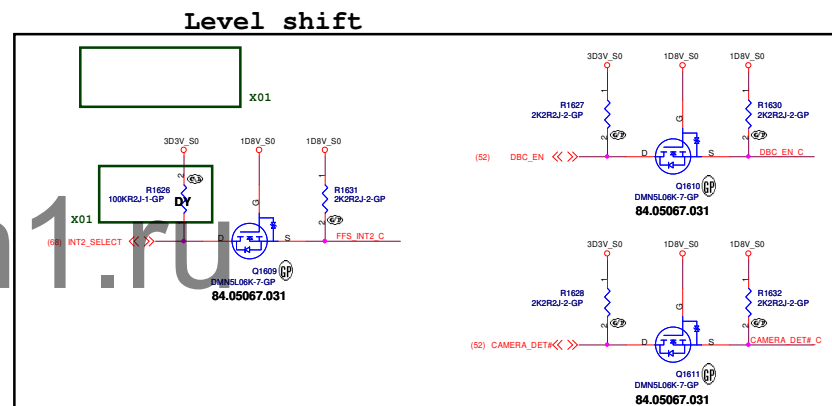
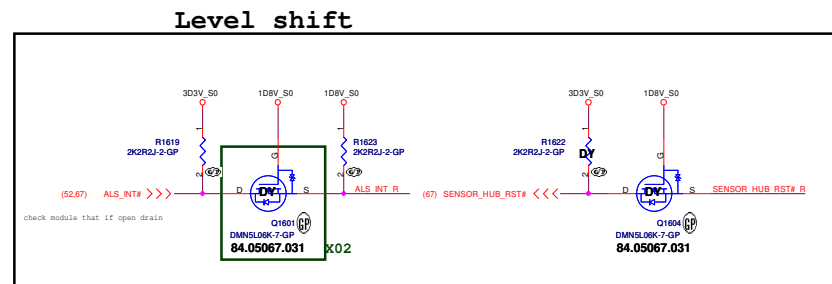
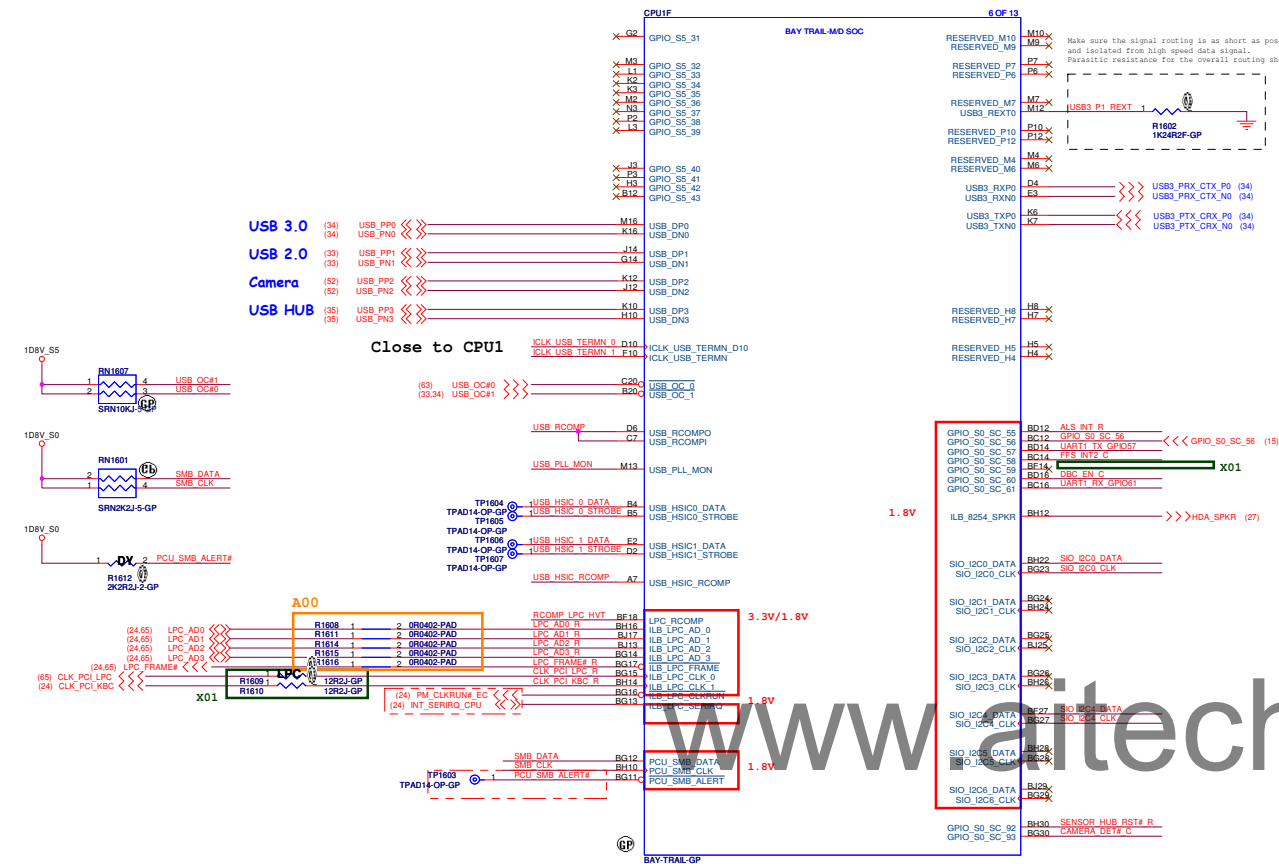
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Title: **CPU(STRAP)**

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SSID = PCH



Port		Type	Device	Address (Write/Read)
PCH	SMB_CLK/SMB_DATA	Master	Touch pad	0x58 / 0x59
			SODIMM	0xA0
			Free Fall Sensor	0x32 / 0x33

$$V_{GS}(th) = 1V$$

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Title	
CPU (USB/LPC/GPIO)	
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SSID = PCH

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Title

CPU (DMI/FDI/PM)

Size
A4

Document Number

Rev
A00

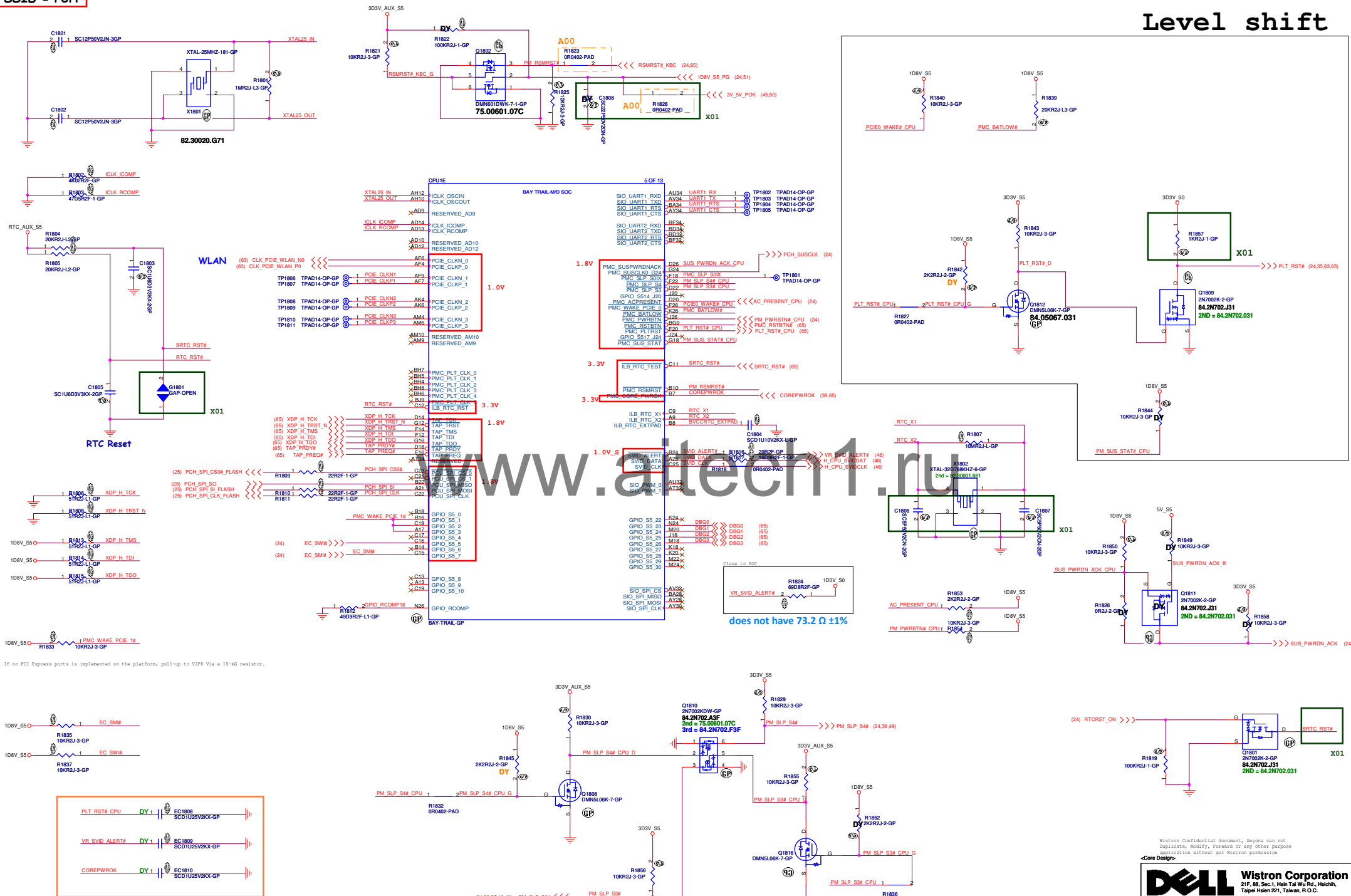
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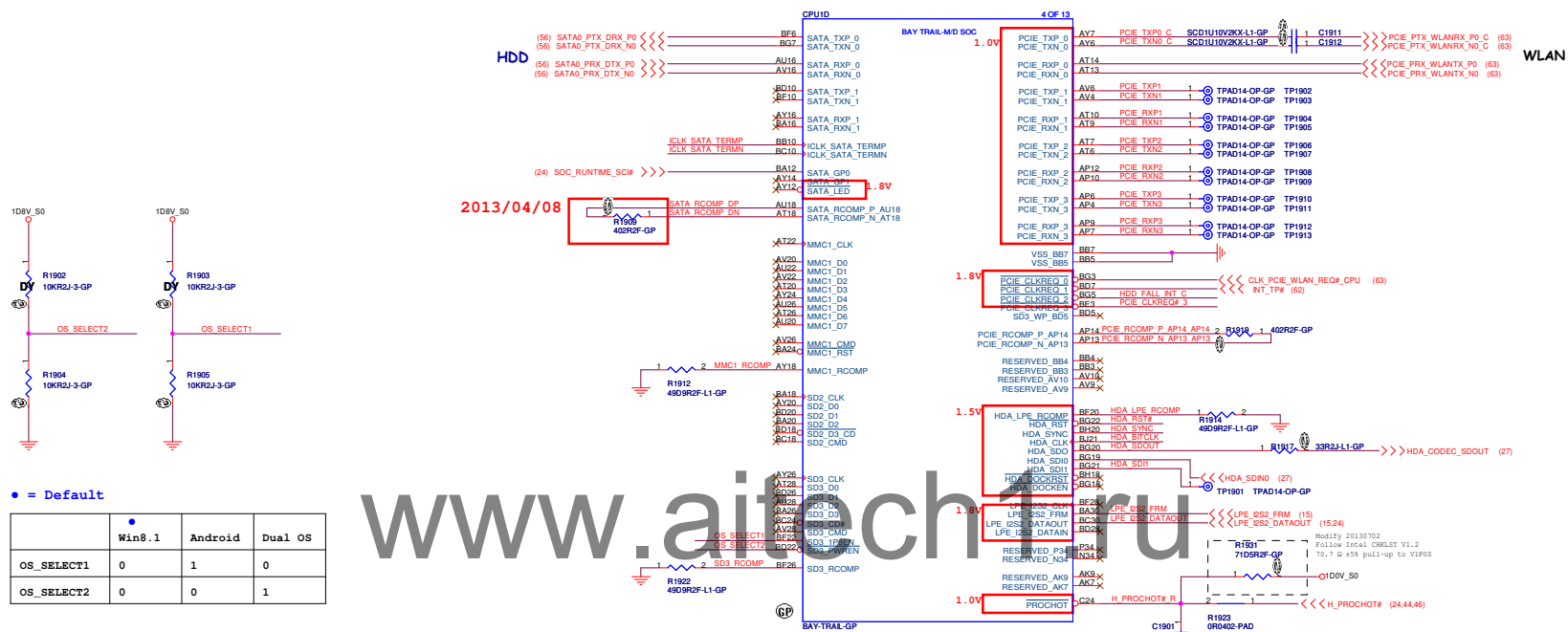
SSID = PCH

Level shift

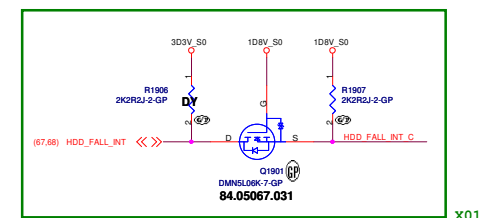
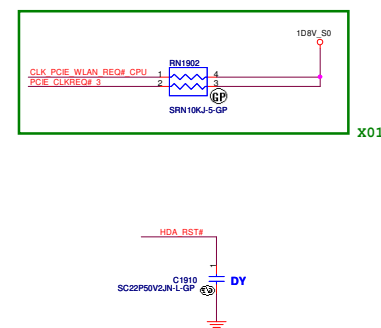
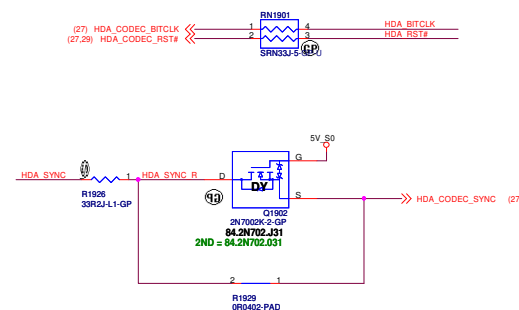
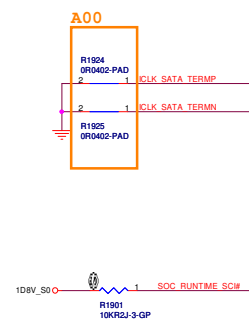


reserve the 0402 0.1u caps on reset for EMI

SSID = PCH



	Win8.1	Android	Dual OS
OS_SELECT1	0	1	0
OS_SELECT2	0	0	1




SSID = PCH

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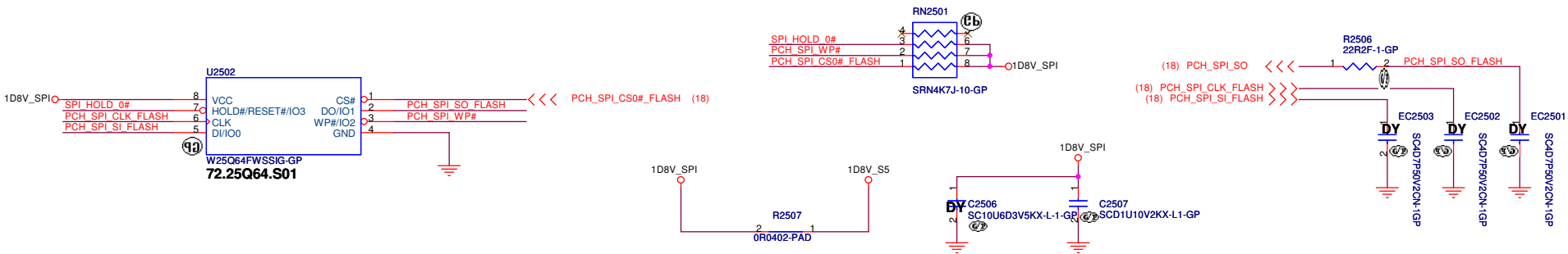
SSID = PCH

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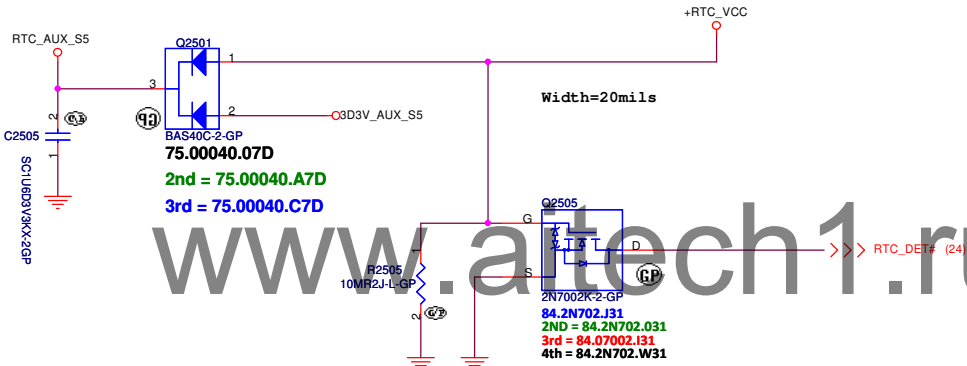
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SPI FLASH ROM (8M byte) for PCH

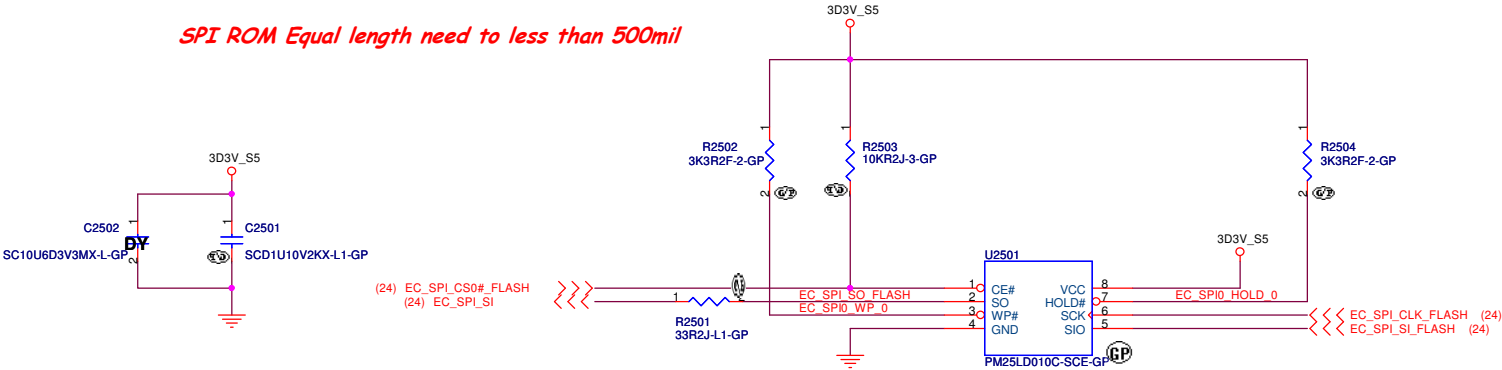


SSID = RBAT



SPI FLASH ROM (128k byte) for EC

SPI ROM Equal length need to less than 500mil

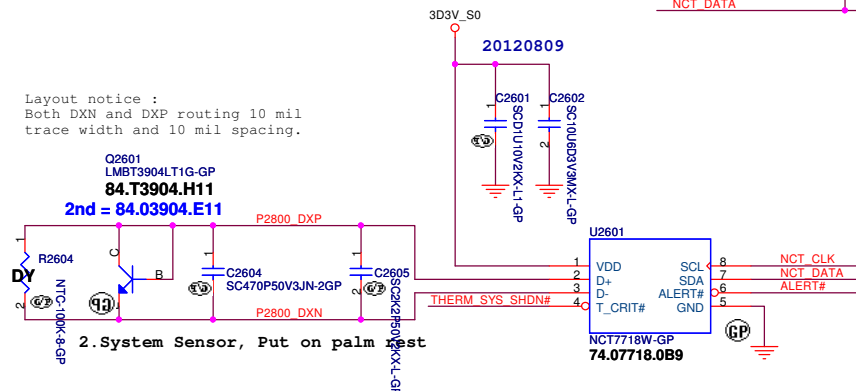


72.25010.N01

SSID = Thermal

Thermal sensor NCT 7718W

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.



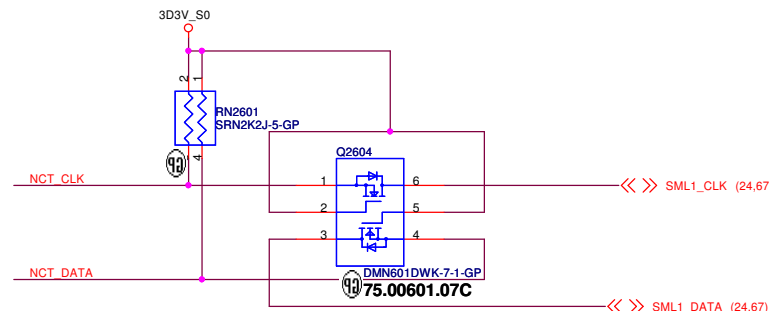
1.H/W T8 Shutdown

ALERT# /T CRIT#
Pull-up Resistor

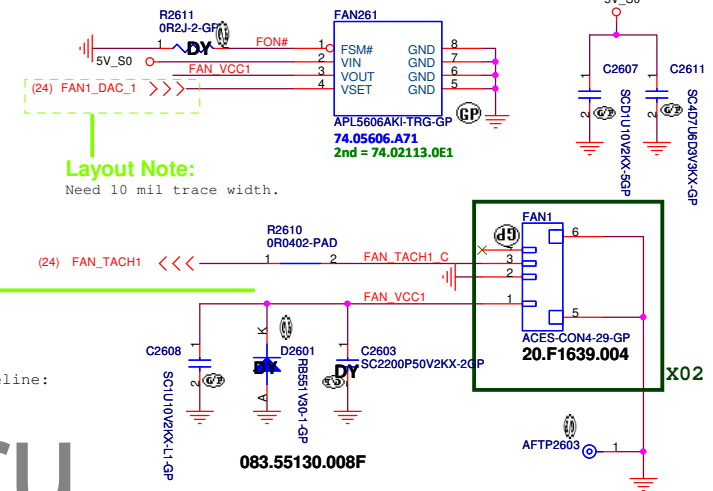
R5	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

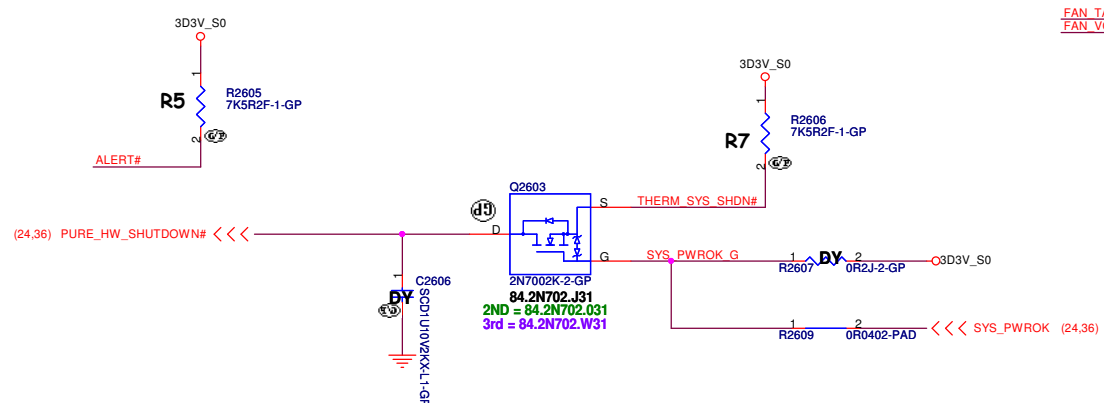
T8=89 degree



Layout 15 mil
Fan controller1



Layout Note:
Signal Routing Guideline:
Trace width = 15mil

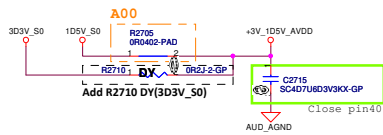
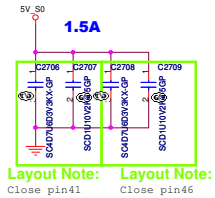
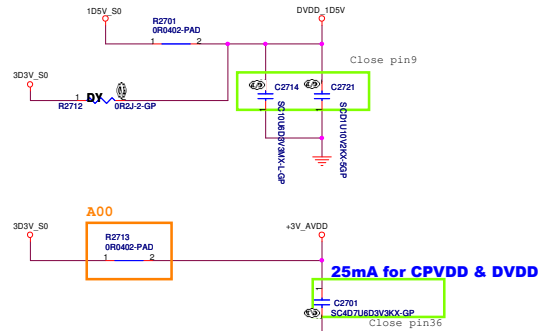


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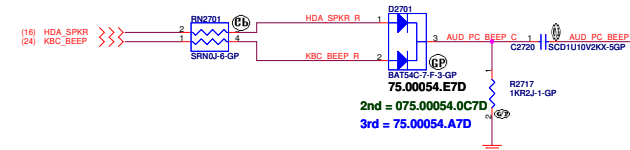
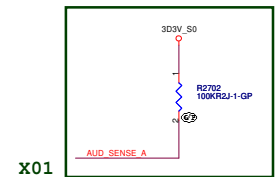
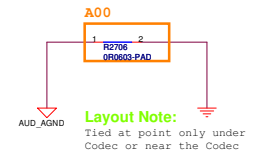
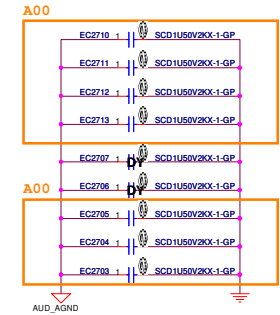
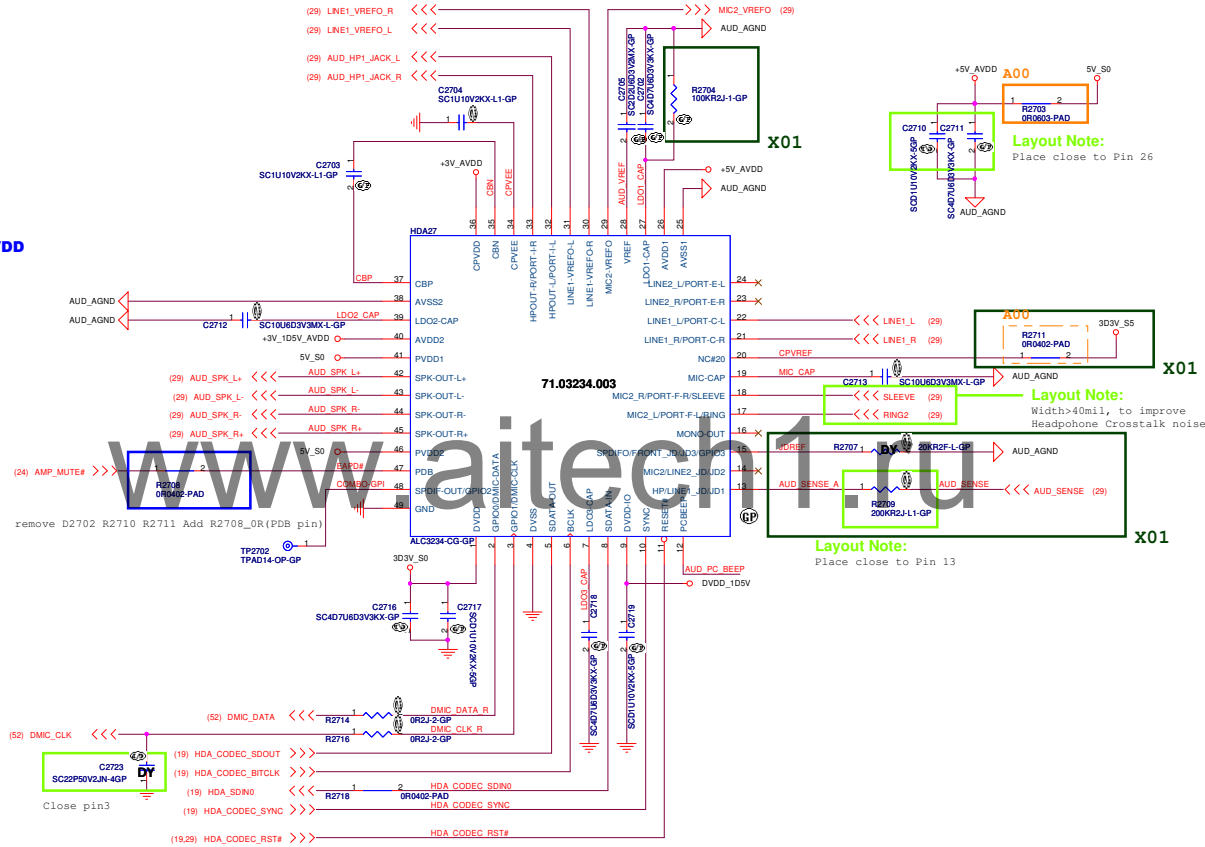
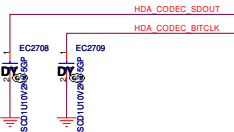
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Title Thermal 7718/Fan Controller P2793			
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SSID = AUDIO



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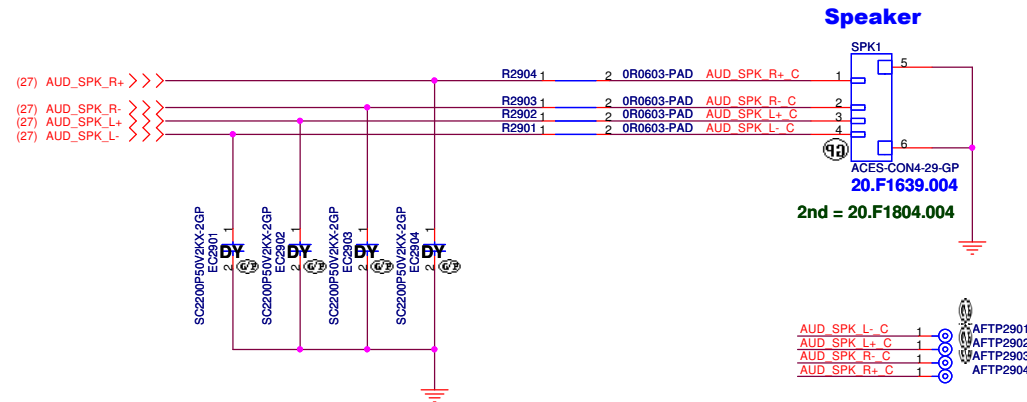
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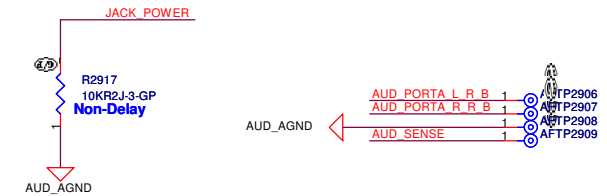
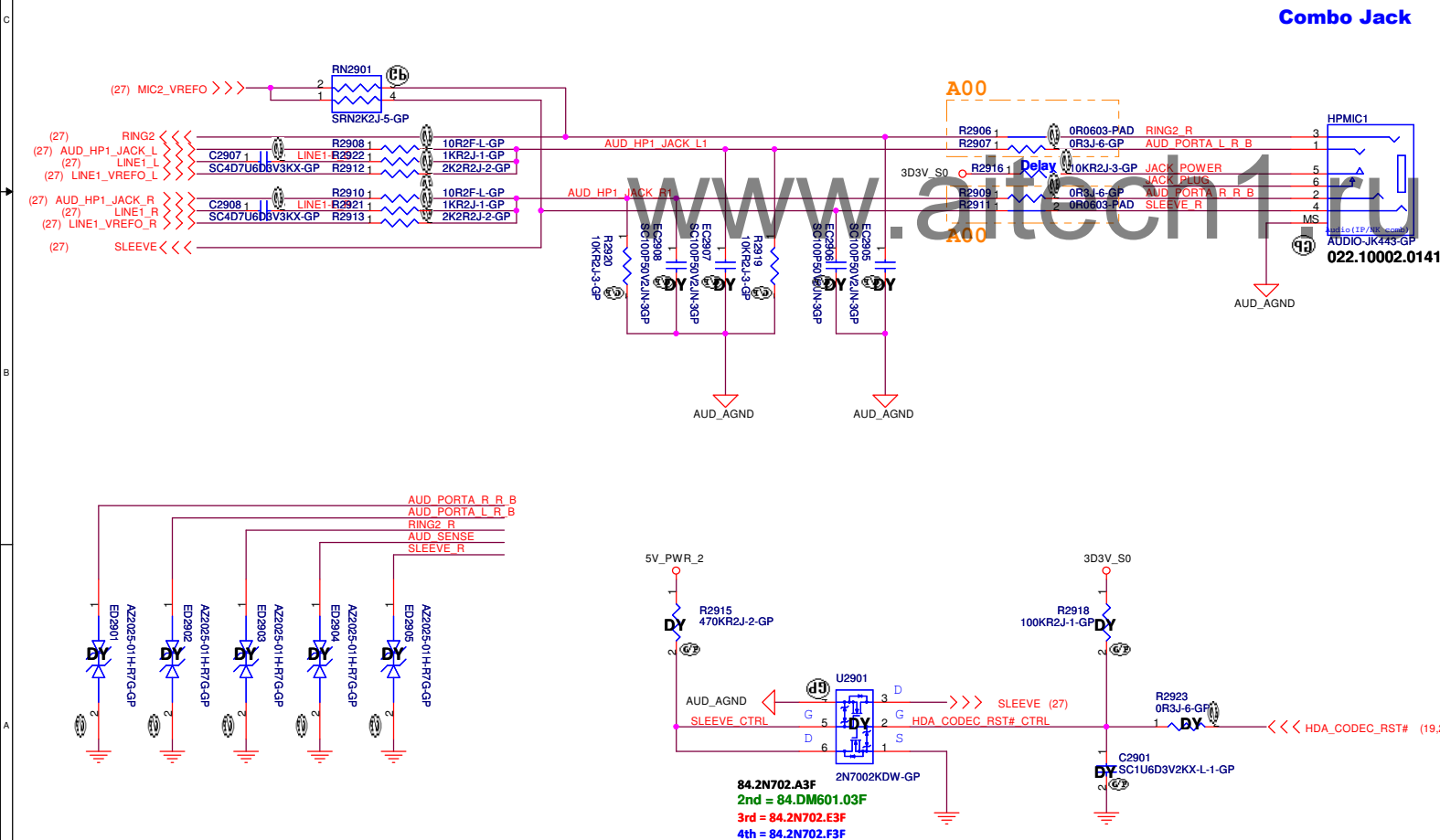
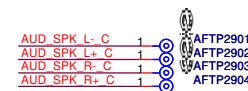
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Size	Document Number				Rev
A4	Redwood 11.6"				A00
Date: Tuesday, April 01, 2014		Sheet 28		of 102	

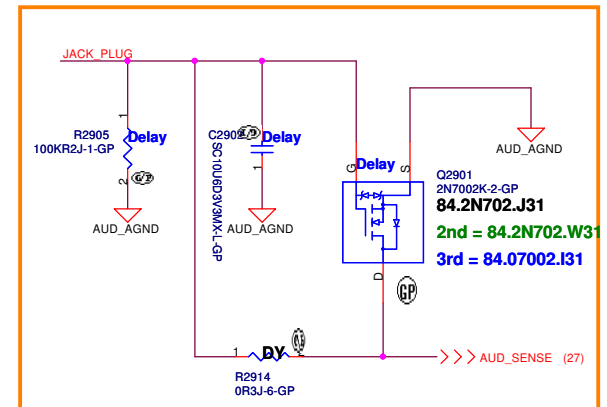
SSID = AUDIO



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



Delay circuit



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Title			
Audio Jack			
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Size A4	Document Number Redwood 11.6"		Rev A00
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SSID = LAN

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Rev

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Date: Tuesday, April 01, 2014

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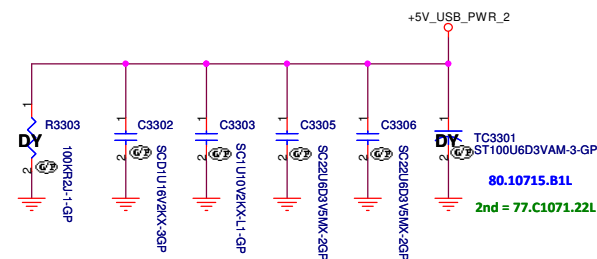
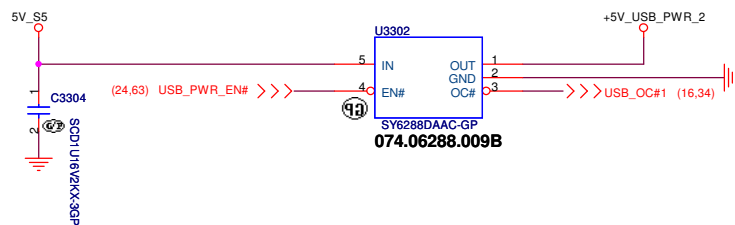
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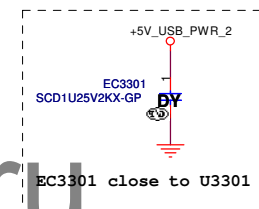
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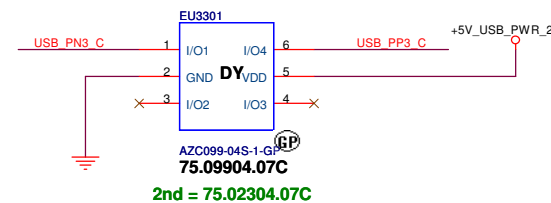
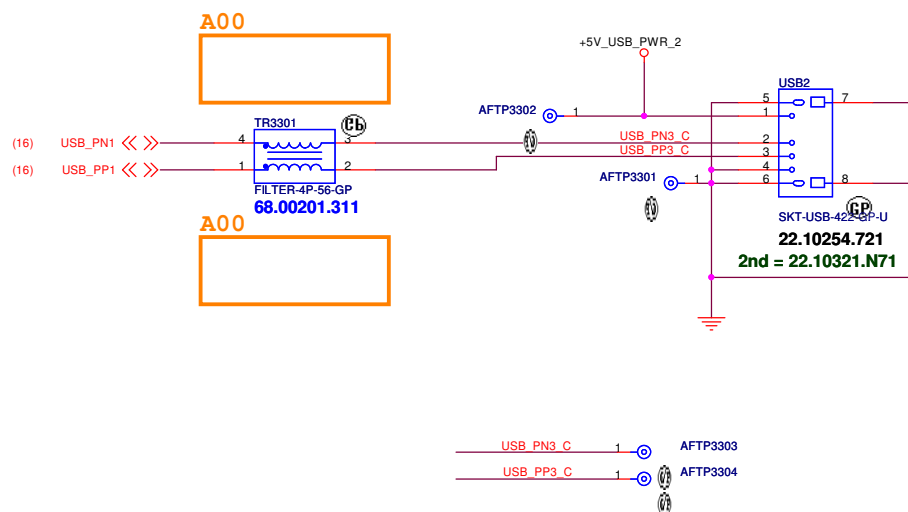


USB Power SW

Vendor	Vendor P/N	Wistron P/N	Priority	Rate current
SILERGY	SY6288DAAC	074.06288.009B	1ST	2A Low Active
GMT	G524B2T11U	074.00524.0C9F	2ND	2.5A Low Active



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Title

USB 2.0 Port

Size
A3

Document Number

Redwood 11.6"

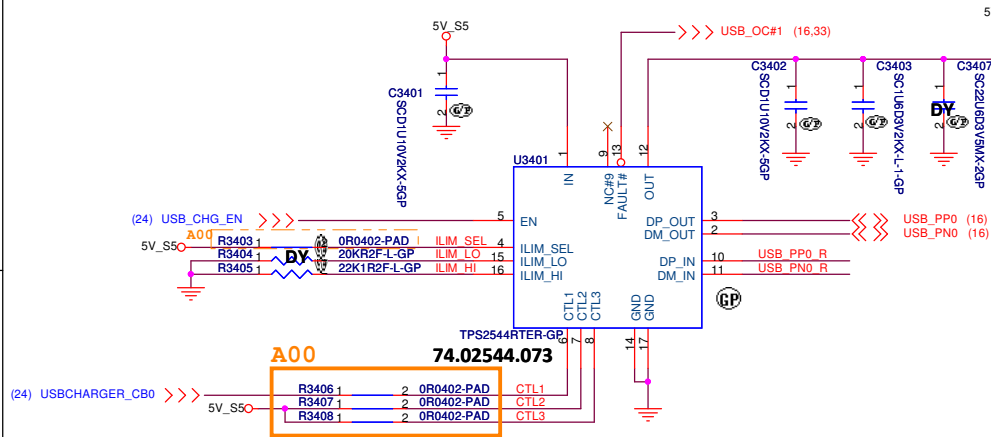
Rev

A00

Date: Tuesday, April 01, 2014

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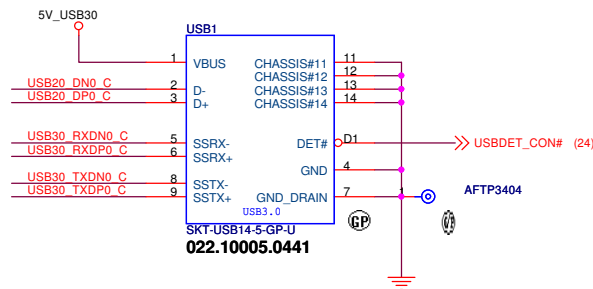
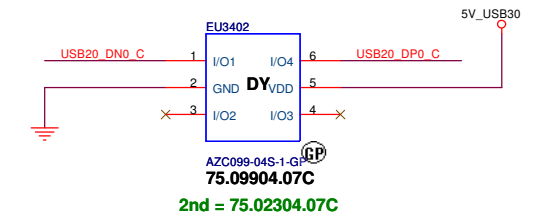
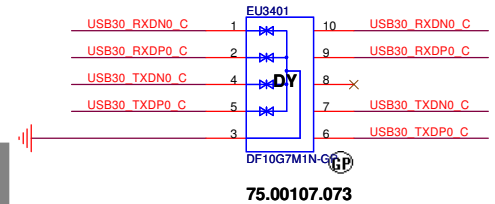
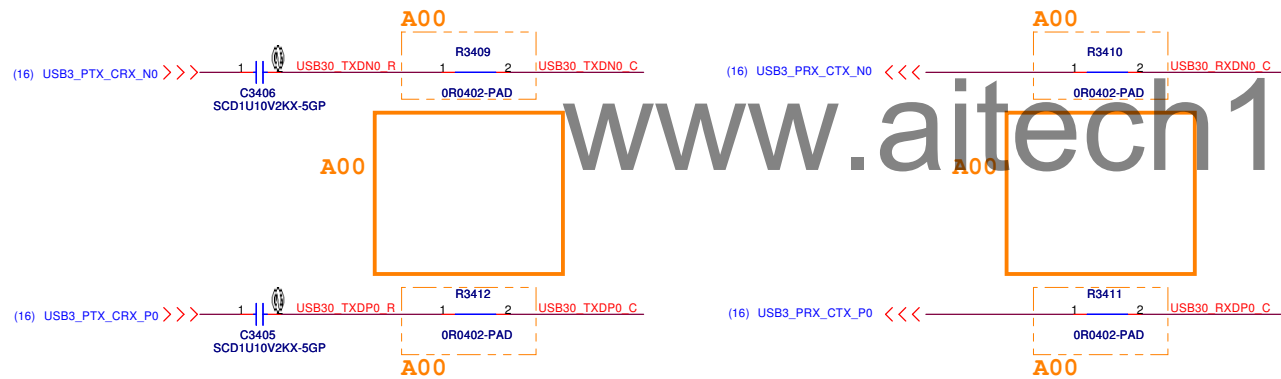
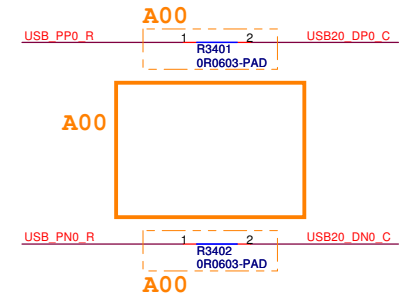
USB Charger



If MLCC is used as Main Source.
Inform Layout team to remark Pin 1 as positive.
In case MLCC shortage and other type of Cap With Polarity Is Used.

Device Control Pins

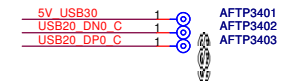
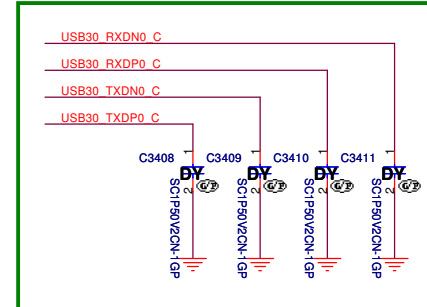
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X



USB 3.0 Connector Pin definition

Pin	Definition
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+ SuperSpeed RX
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+ SuperSpeed TX

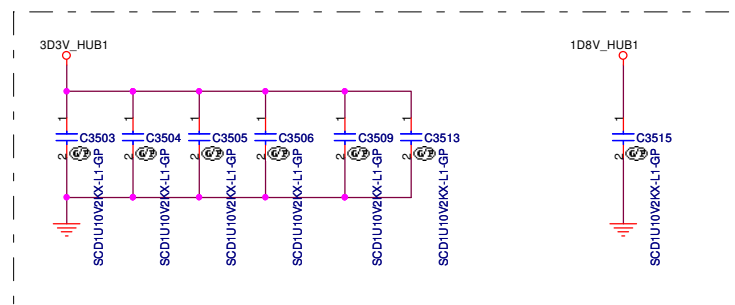
Reserved for RF



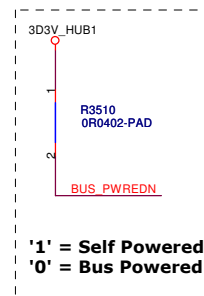
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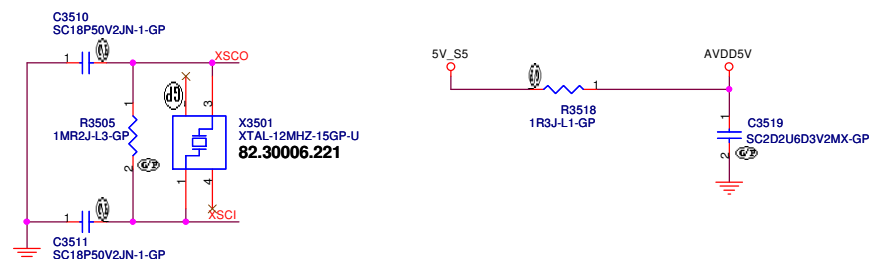
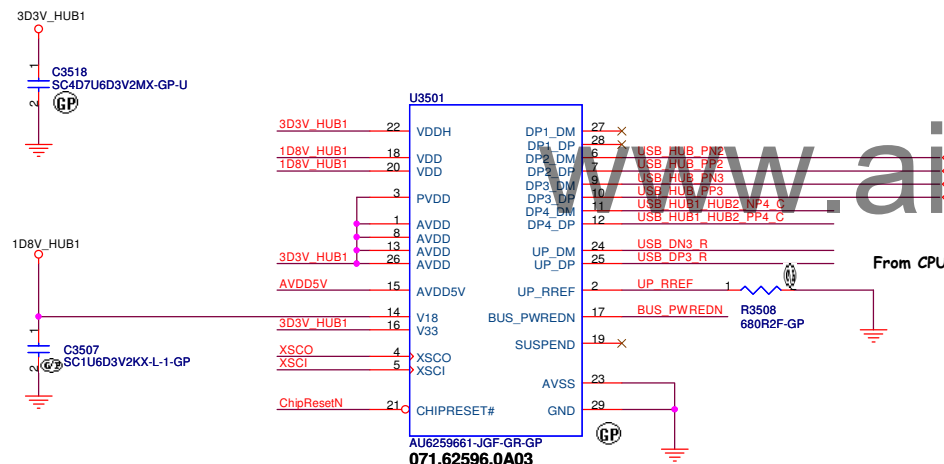
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Size	Document Number	Rev	A00
A3	Redwood 11.6"		
Date:	Tuesday, April 01, 2014	Sheet	34 of 102



Near the chip side.

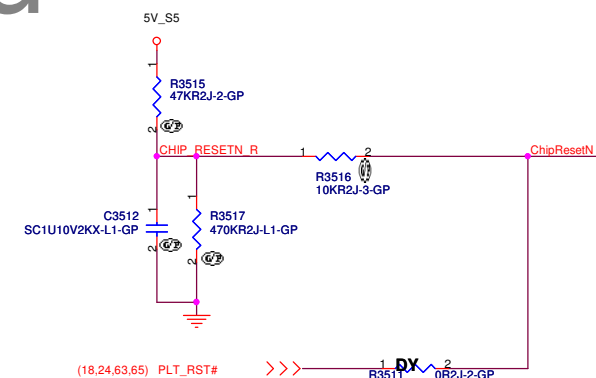


'1' = Self Powered
'0' = Bus Powered



USB Table

Pair	Device
1	N/A
2	Sensor Hub
3	TOUCH PANEL
4	USB Hub2



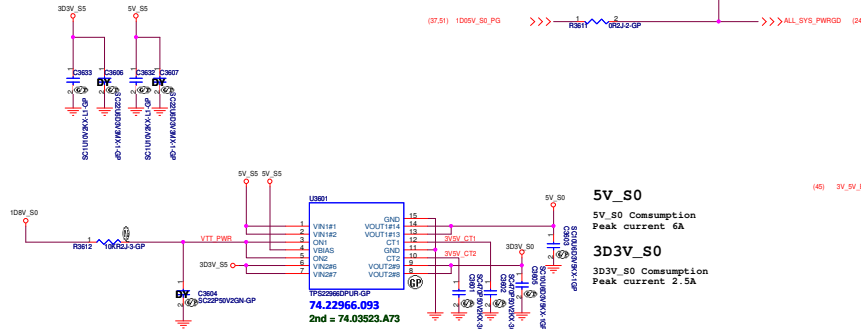
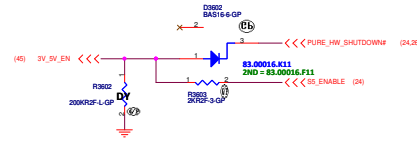
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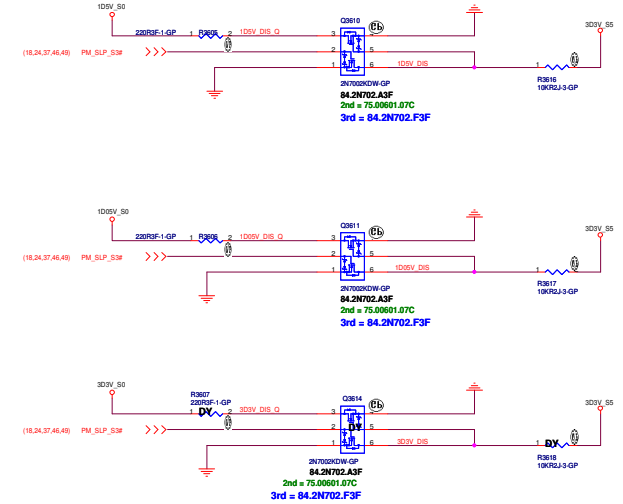
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Title USB HUB			
Size Custom	Document Number Redwood 11.6"		Rev A00
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```
SSID = Reset.Suspend
```

ROSA Run Power

***Power Good***

Discharge circuit



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Power Sequence

DDR3_VCCA_PWRGD

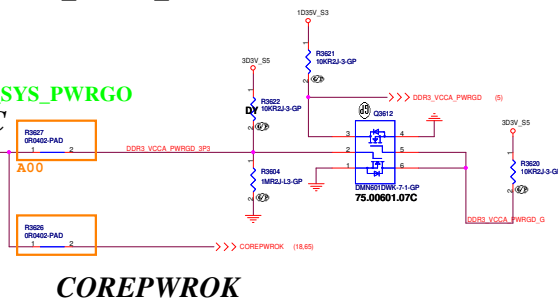
Does not link to SOC!!

Delay 110ms with ALL_SYS_PWRGO

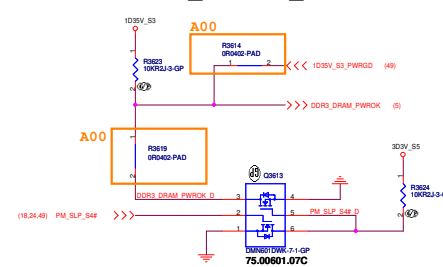
From EC

20130507

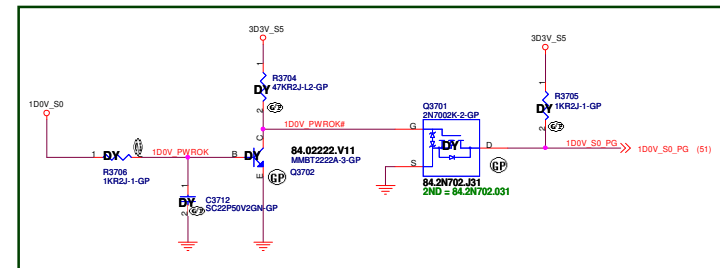
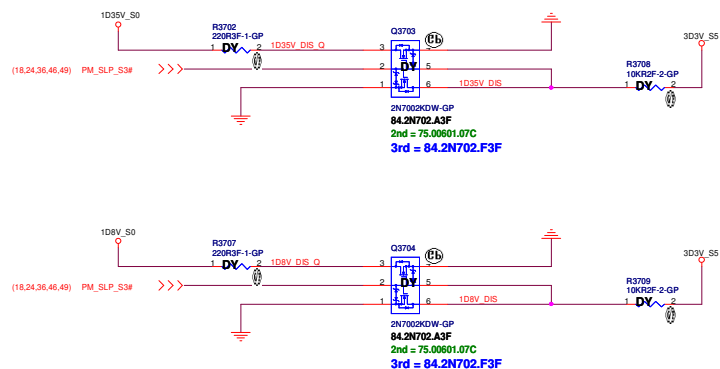
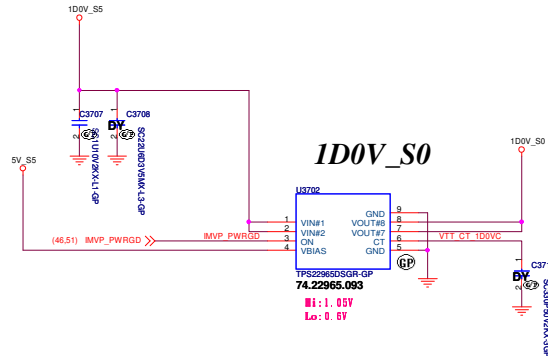
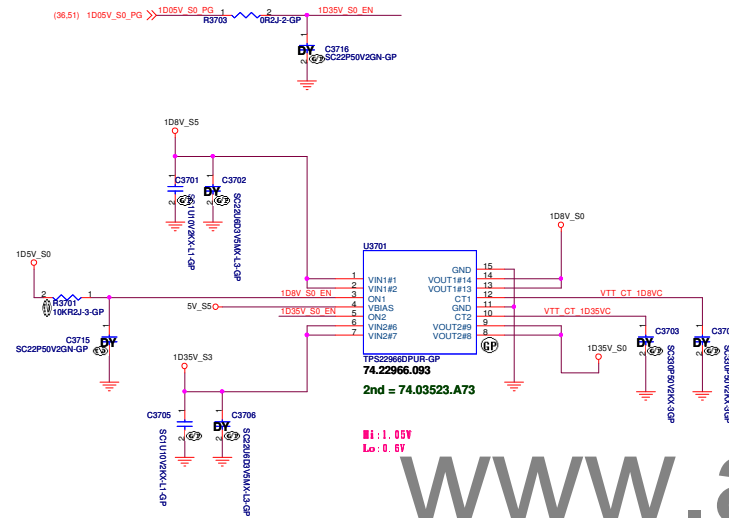
KBC GPIO77
delay ??? total
need KBC to modify!!!



DDR3_DRAM_PWROK



1D35V_S0
1D8V_S0



X01


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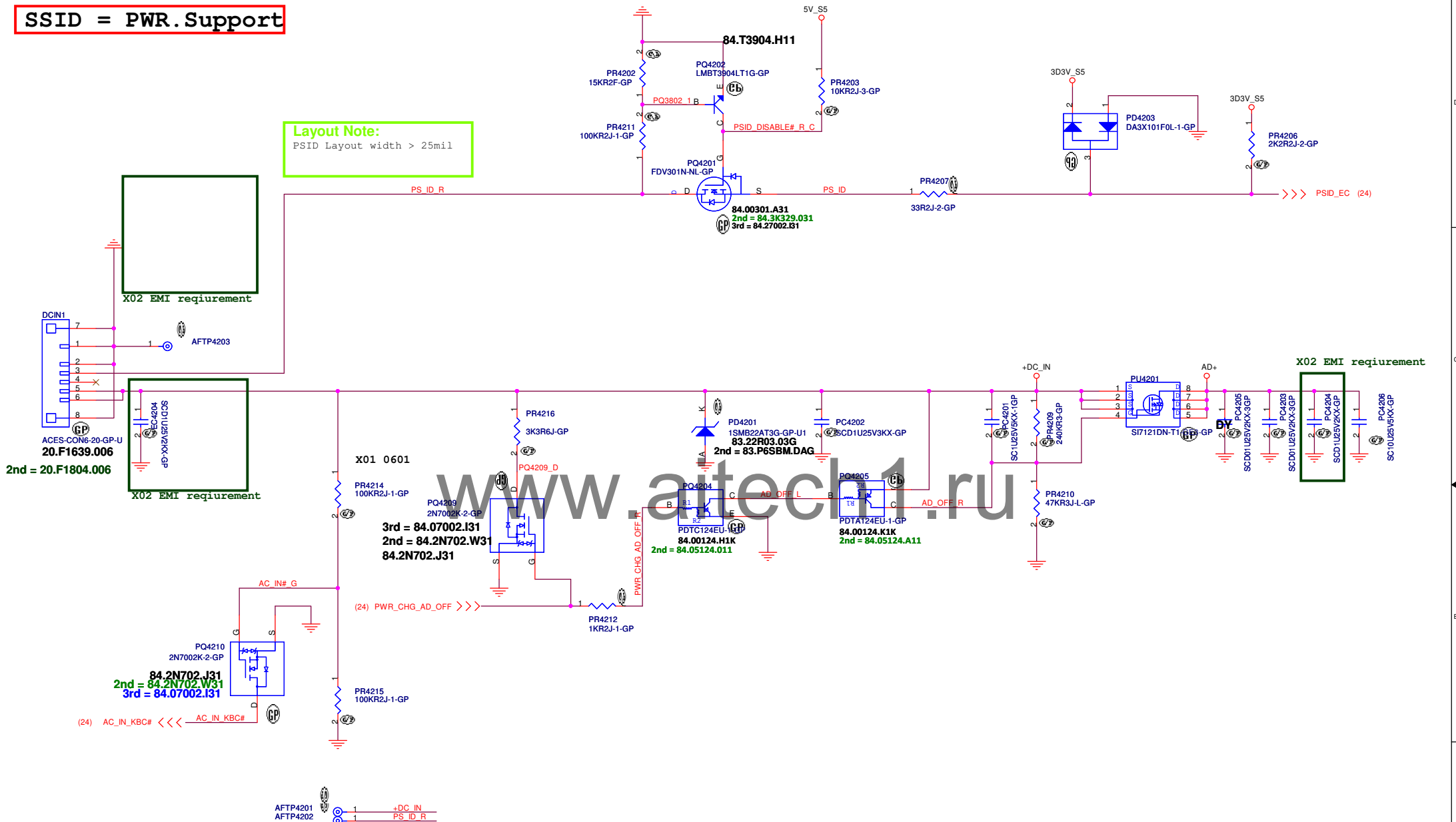
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Date: Tuesday, April 01, 2014

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SSID = PWR.Support

Layout Note:
PSID Layout width > 25mil



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Title

DCIN JACK

Size
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Document Number

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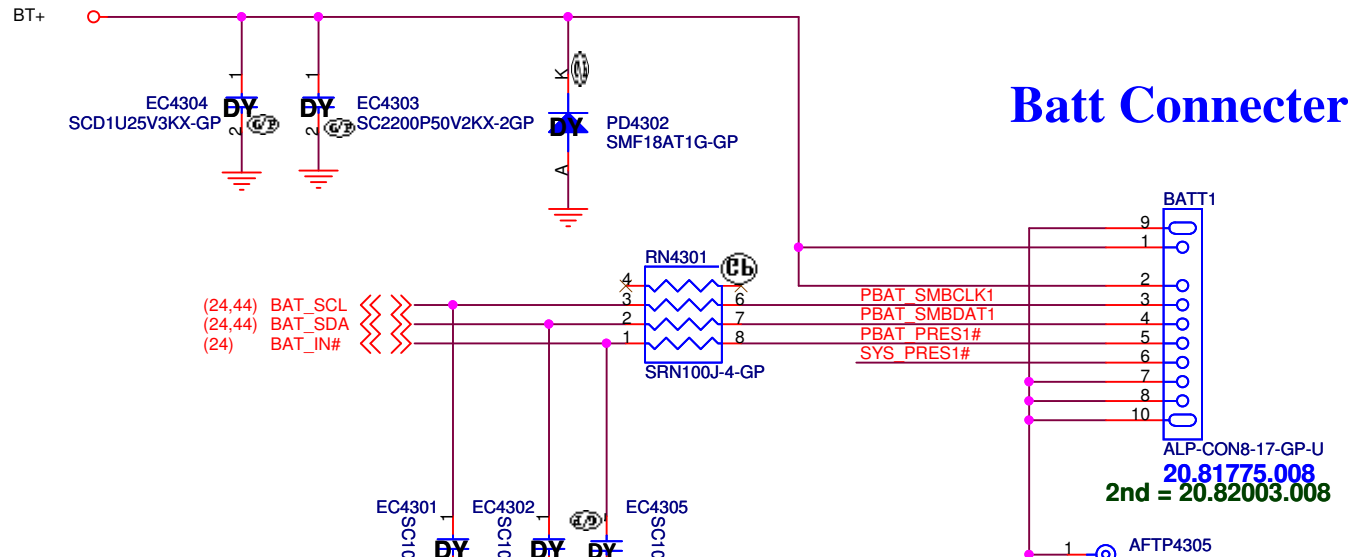
Rev

A00

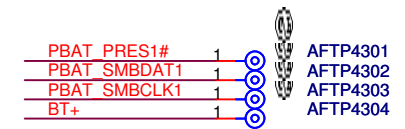
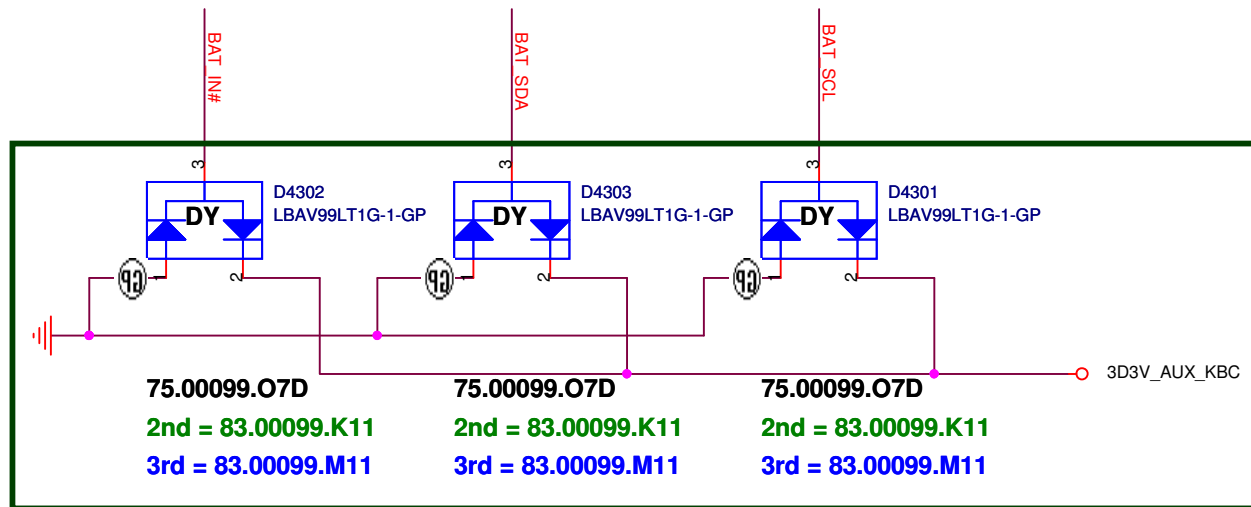
Date: Tuesday, April 01, 2014

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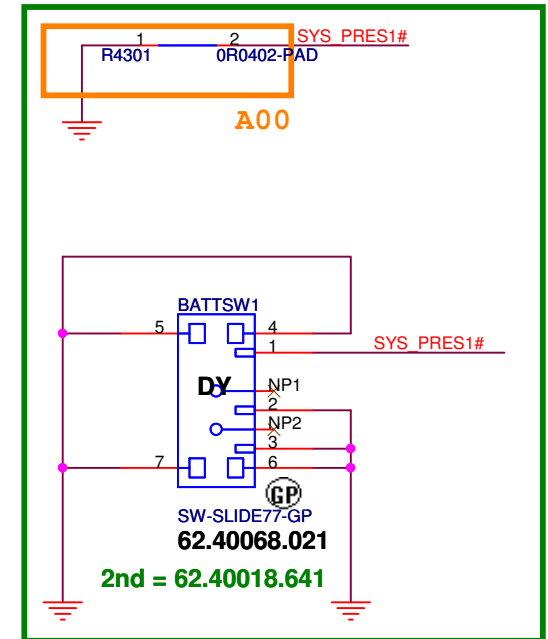
SSID = PWR.Support



Placement: Close to Batt Connector



X02



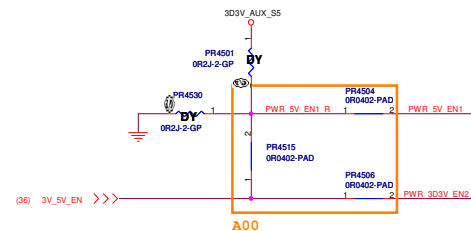
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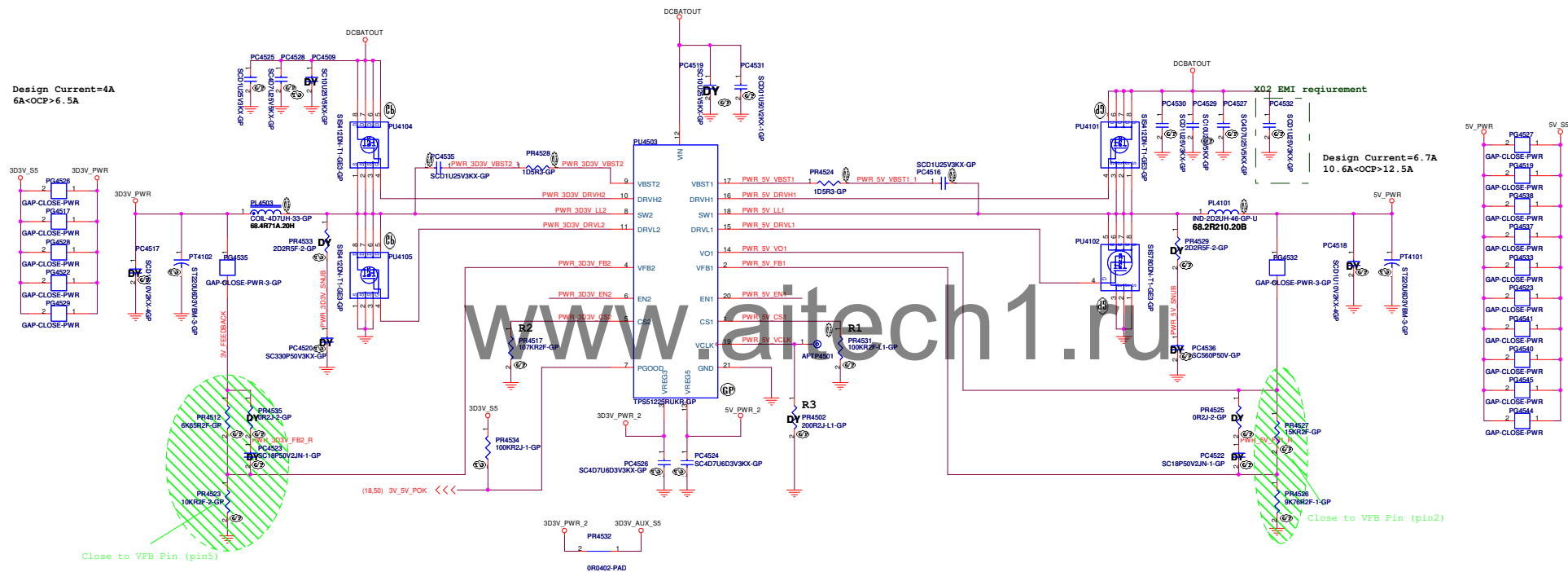


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```
SSID = PWR.Plane.Regulator_5v3p3v
```



Design Current=4A
6A<OCP>6.5A



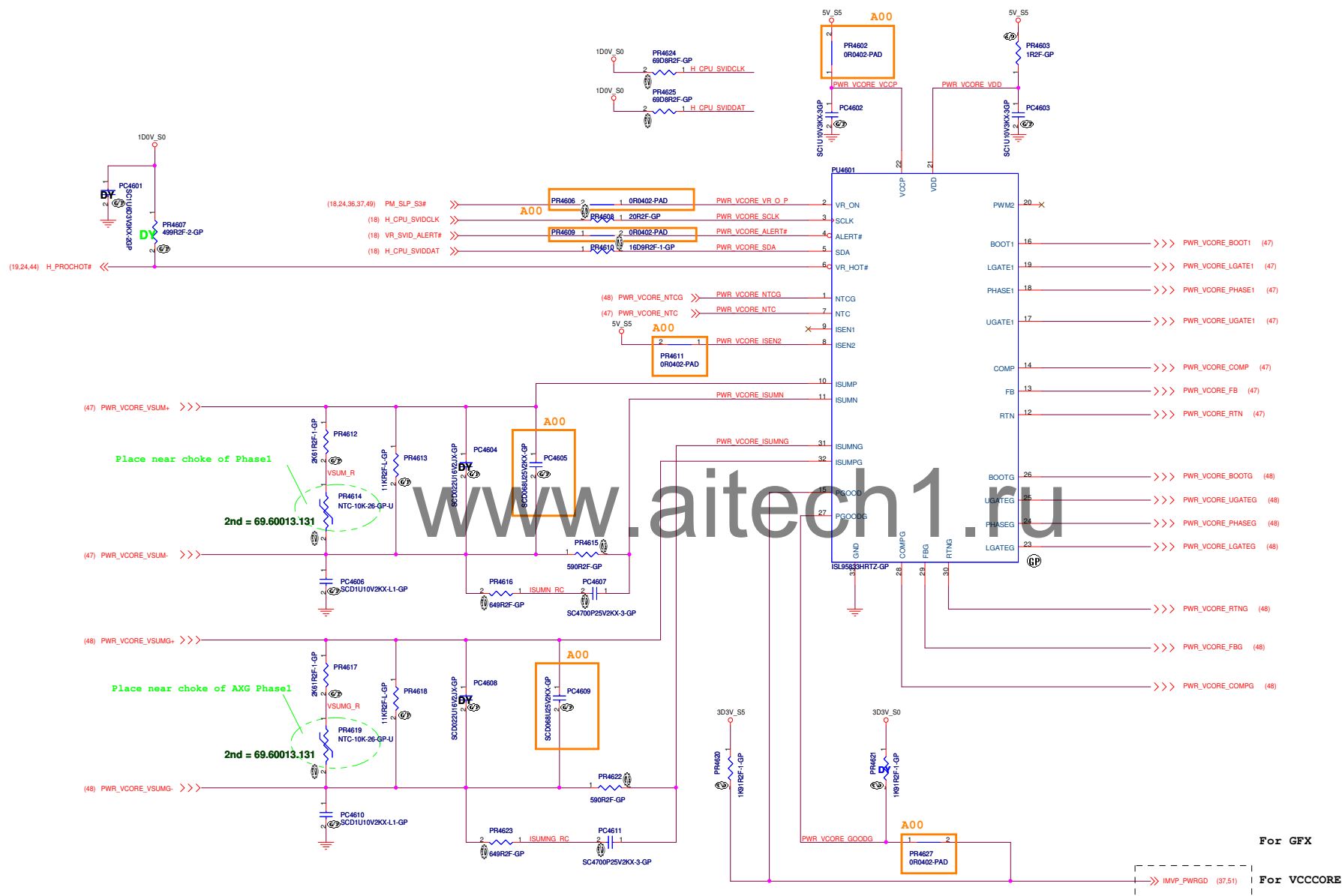
I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 4.7UH PCB0603T-4R7MS Cyntec 28mhm/33mhm Isat =6.5Arms 68.4R71A.20H
O/P cap:CHIP CAP T 220U 6.3V M3528 PSL /NEC/ 28mhm / 77.C2271.45L
R/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.0412.037
L/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.0412.037

TPS51225 & TPS51285 Co-lay

	TPS51225	TPS51285
R1	100K	20K
R2	107K	21.5K
R3	DY	200

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap:CHIP CAP L 220V 6.3V M3528 PSL /NEC/ 25mOhm / 77.C271.45L
H/S:SI5412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SI5780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00708.037

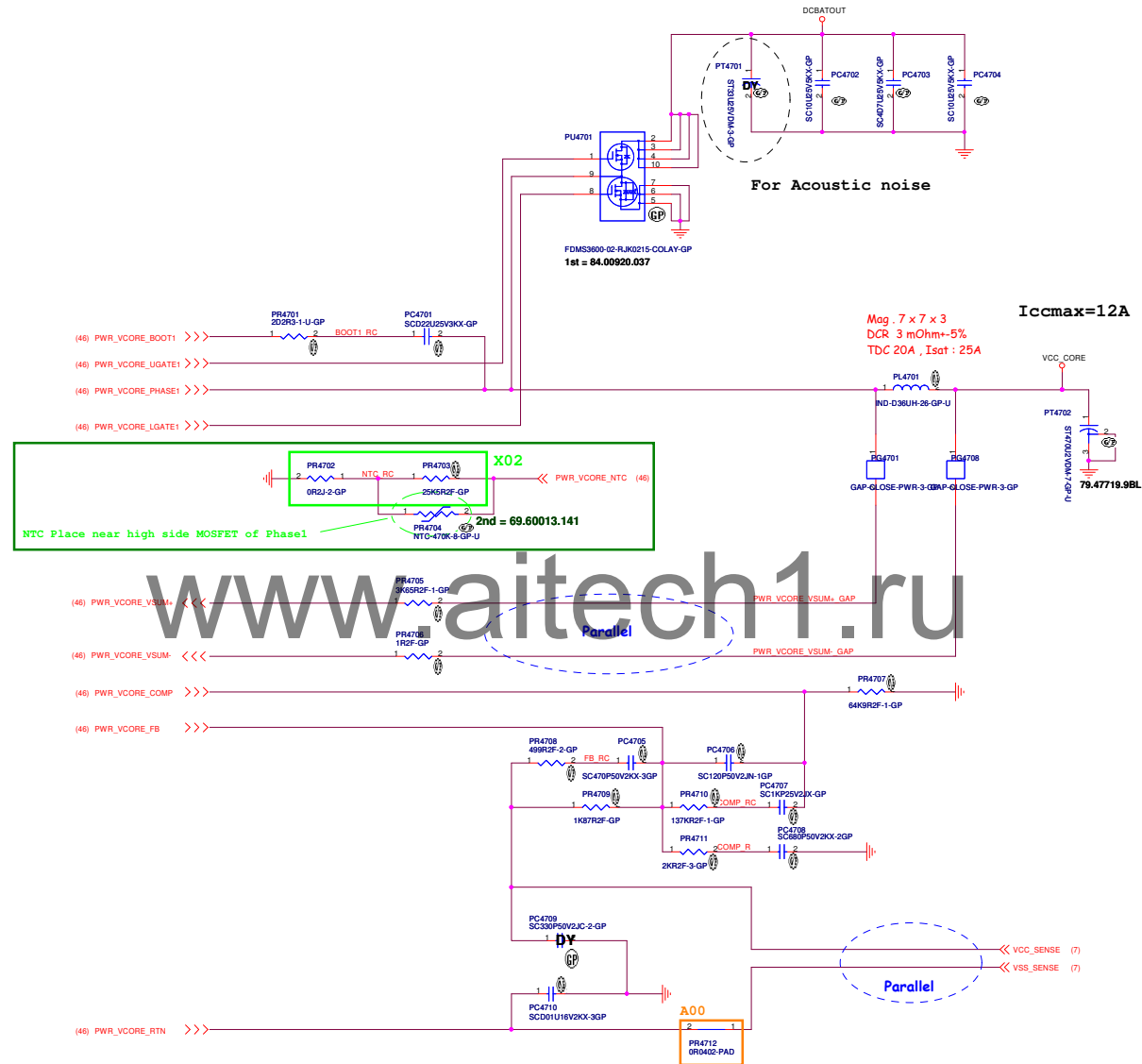
SSID = CPU.Regulator



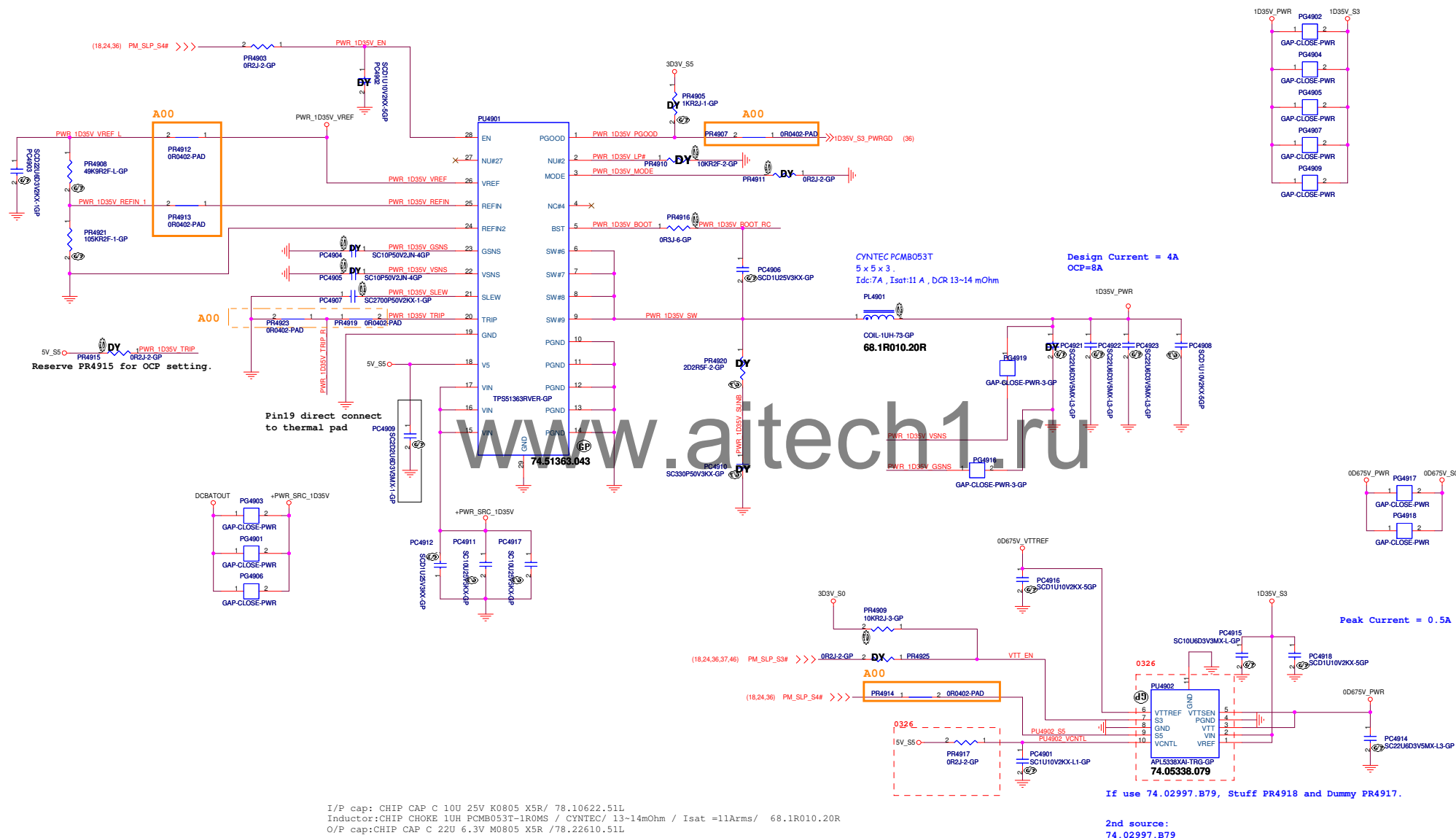
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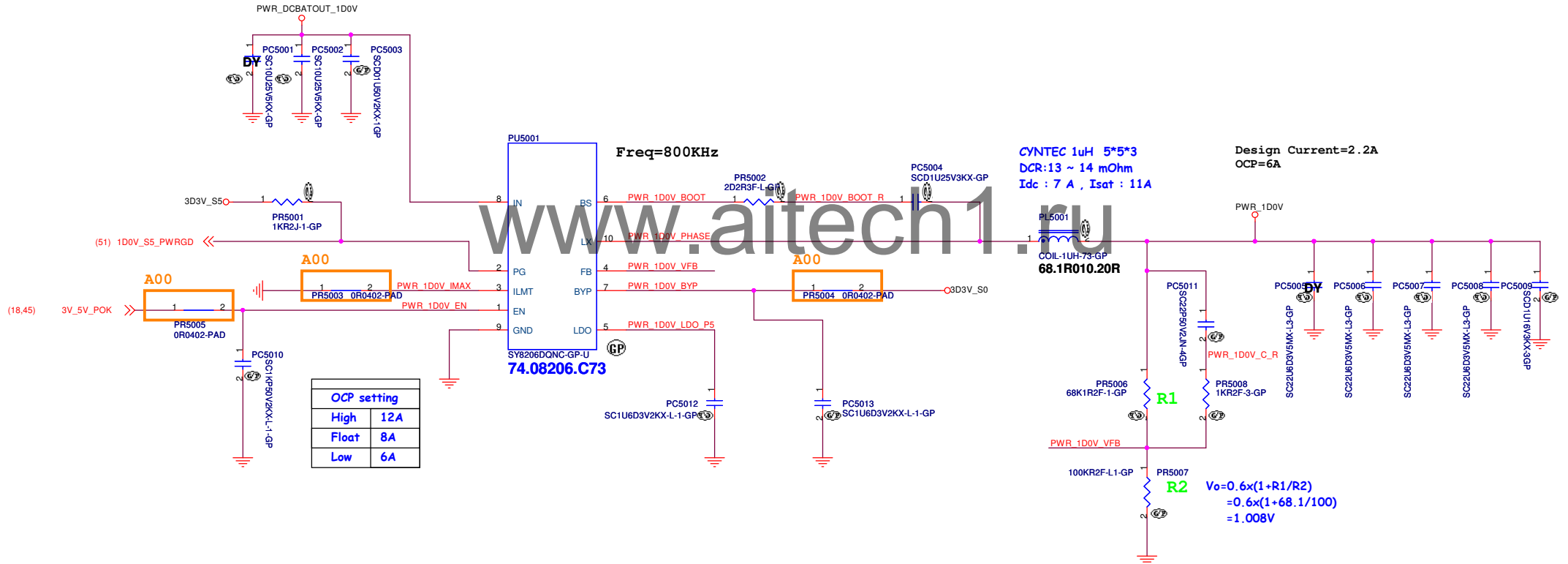
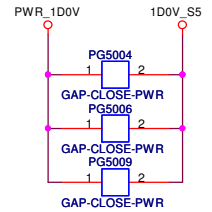
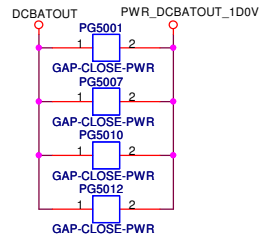
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 Size: C Document Number: **Redwood 11.6"** Rev: **A00**
 Date: Tuesday, April 01, 2014 Sheet 46 of 102



SSID = PWR.Plane.Regulator_1p35v0p675v



SY8206D for 1D0V



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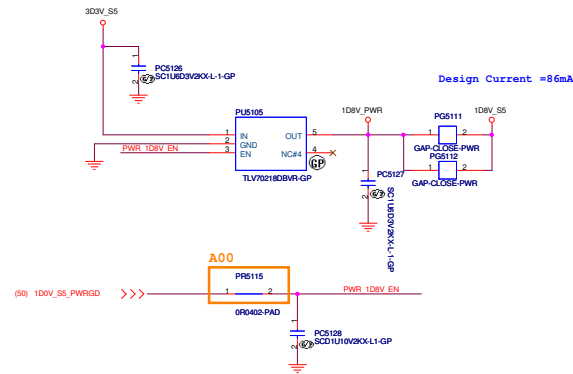


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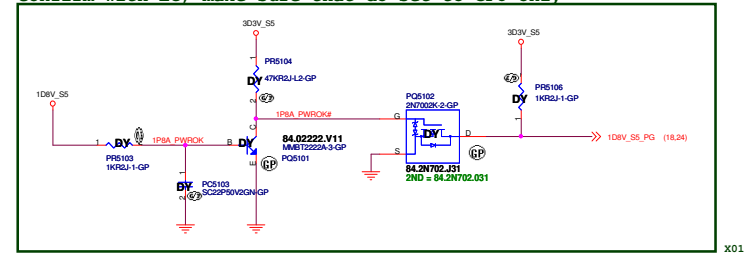
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Size	Document Number	Rev		A00
A3	Redwood 11.6"			
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SSID = PWR.Plane.Regulator_1p8v

TLV70218 for 1D8V_S5



confirm with EC, make sure that do set to GPO only



TLV70215 for 1D5V_S0

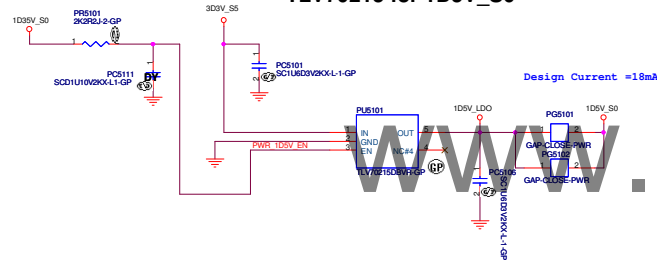
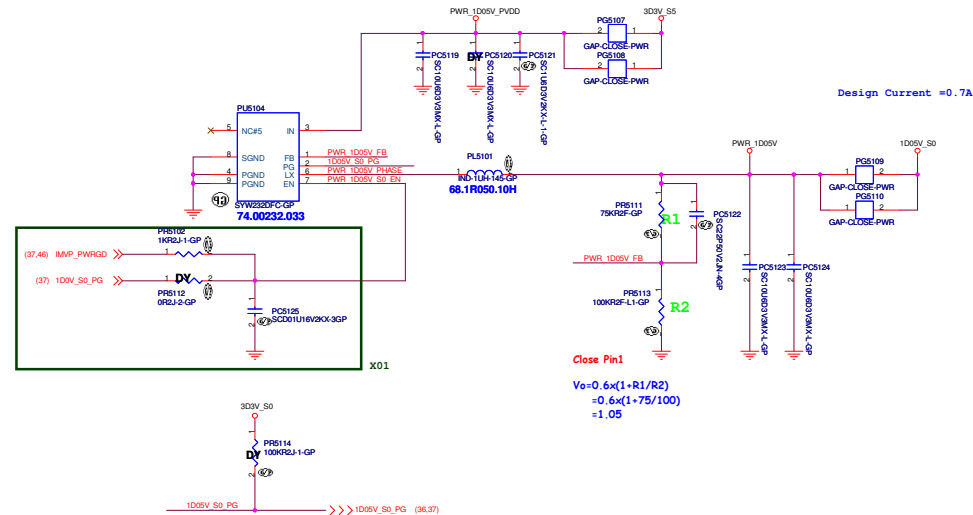


Table 4-12. Cold Boot Timing Spec

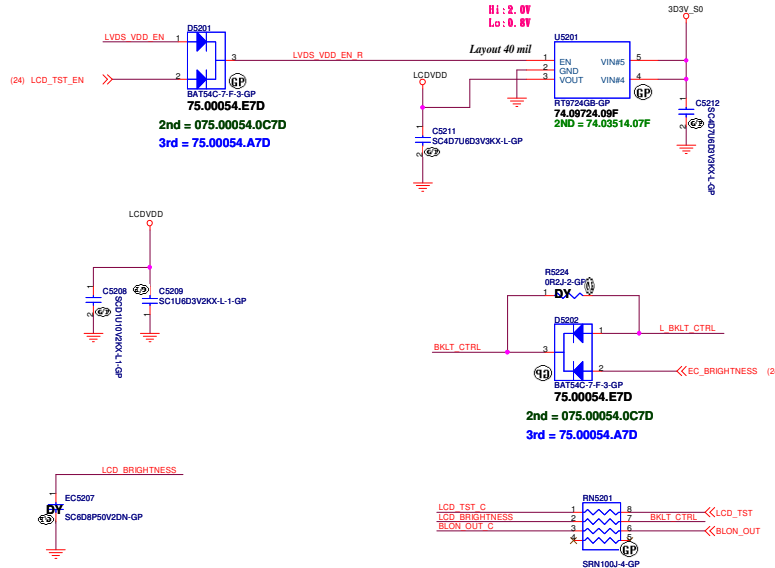
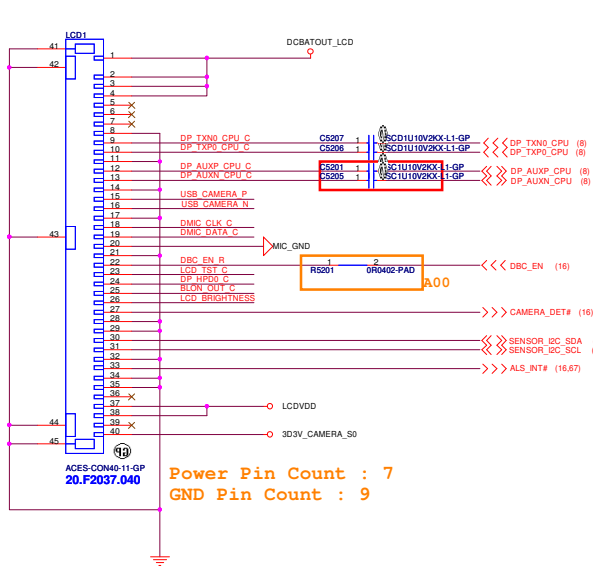
Parameter	Description	Min	Typ	Max	Units
T0	RTC_VCC stable to ILB_RTC_TEST# high	9			ms
T1	VR ramp up time from 10% to 90% voltage level			2	ms
T2	Rail to subsequent rail turn on delay	10		2000	us

SYW232 for 1D05V_S0

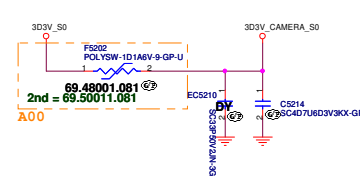


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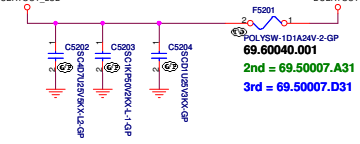
Panel Conn.



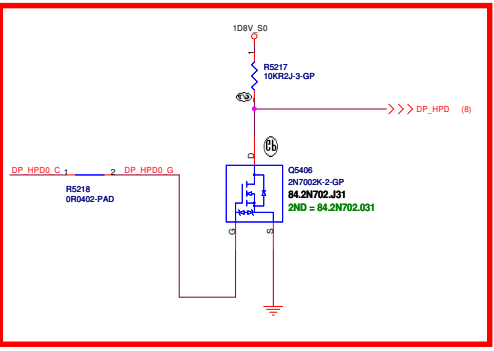
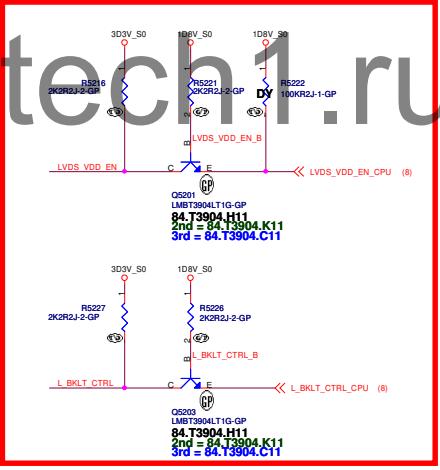
CAMERA POWER



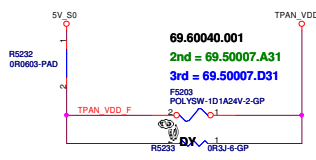
INVERTER POWER



Level shift




TOUCH PANEL POWER



Blanking

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SSID = VIDEO

HDMI Level Shifter & CONNECTOR

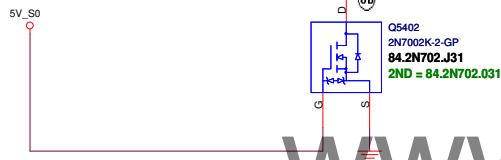
HDMI CONN



Close to HDMI Connector

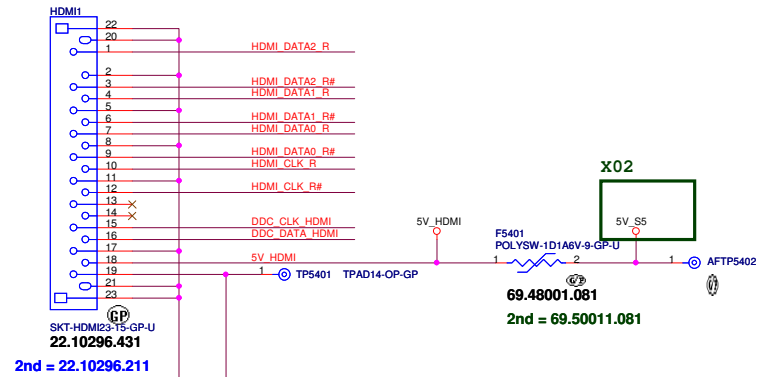
2013/04/10
follow CRB, 619無排阻

Close to Level Shift



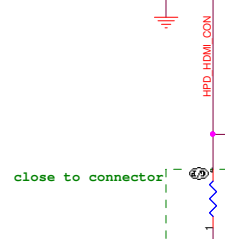
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HDMI_DATA0_R#	DY	R5418	150R2F-4-L-GP	HDMI_DATA0_R
HDMI_DATA1_R#	DY	R5419	150R2F-4-L-GP	HDMI_DATA1_R
HDMI_DATA2_R#	DY	R5419	150R2F-4-L-GP	HDMI_DATA2_R

Reserve 150 ohm bridge resistance
on the HDMI trace as circle for EMI



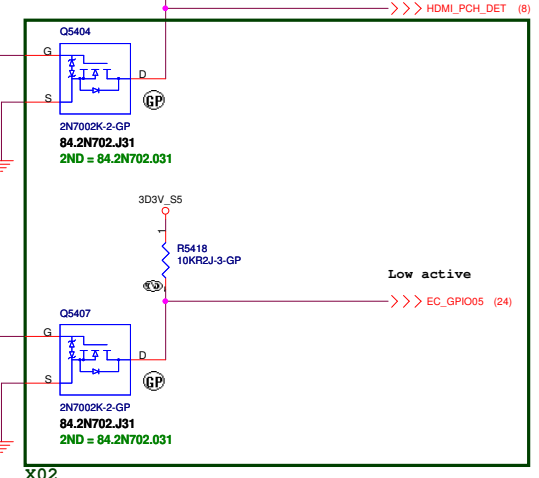
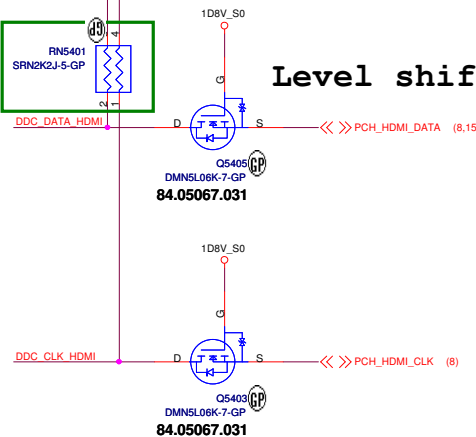
2nd = 22.10296.211

69.48001.081
2nd = 69.50011.081



close to connector

Level shift



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File
HDMI Level Shifter/Connector
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SSID = Display Port

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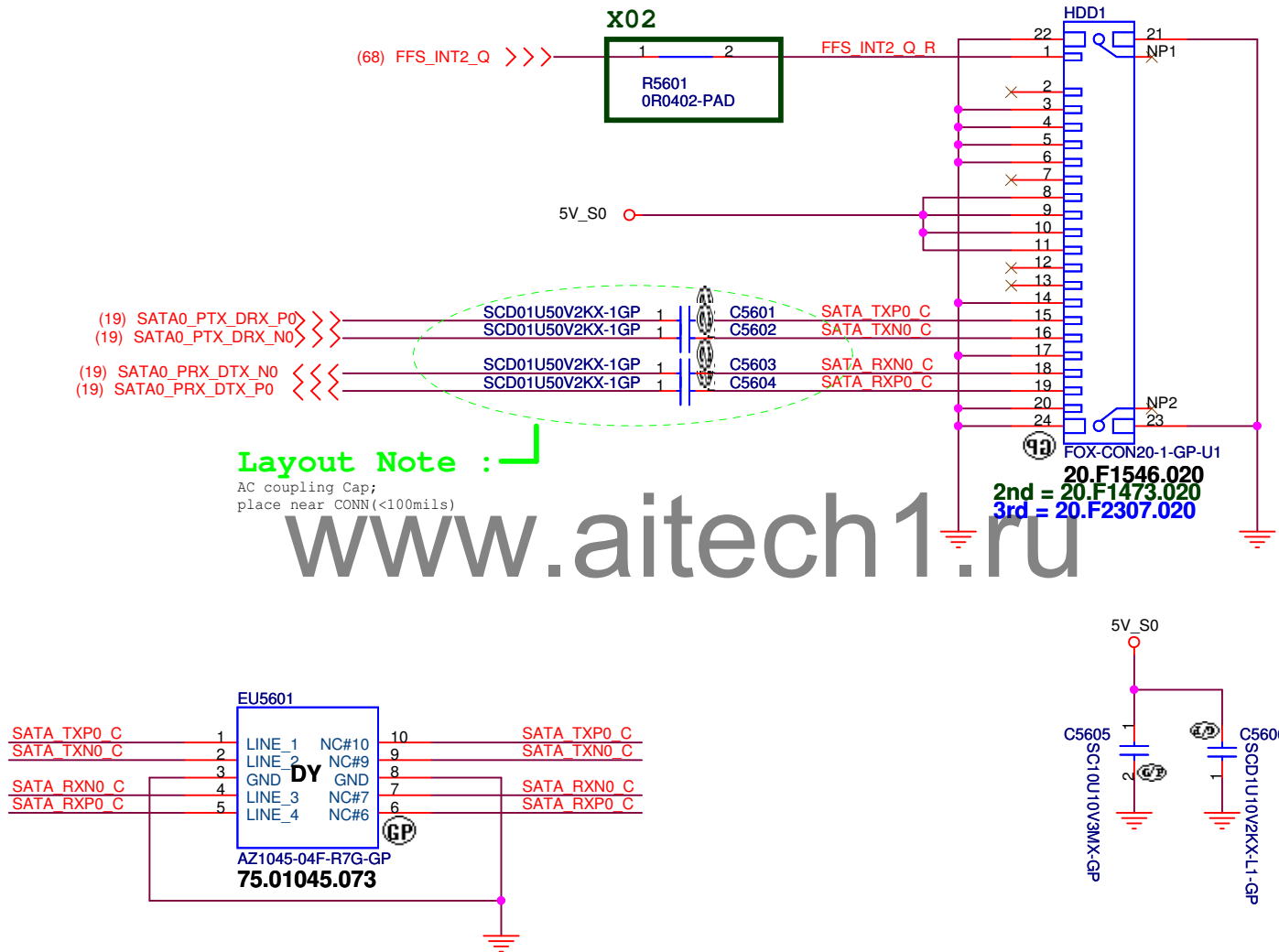
Reserved

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SSID = SATA

SATA HDD Connector



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HDD Connector

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SSID = Wireless

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SSID = 3G

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SSID = mSATA

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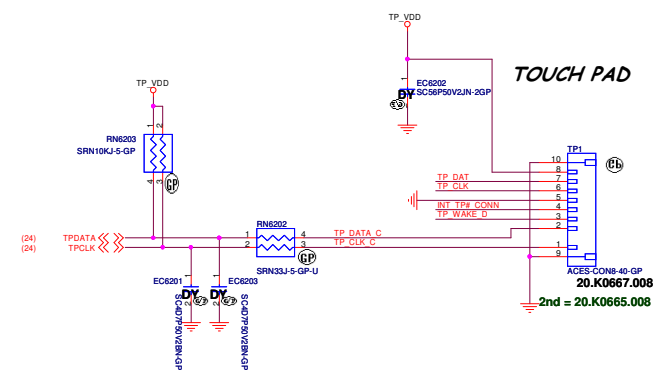
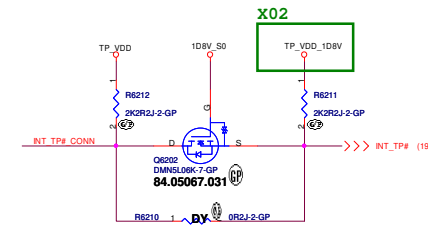
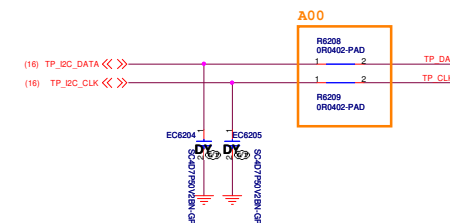
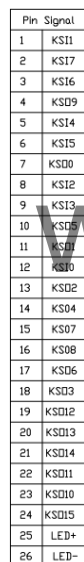
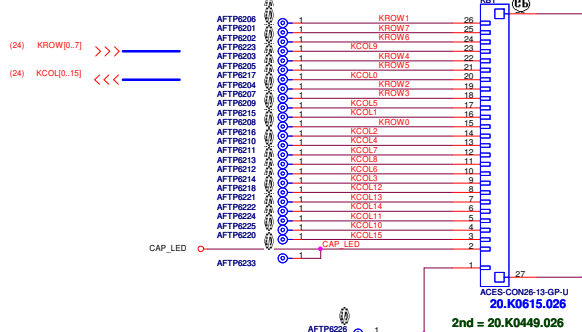
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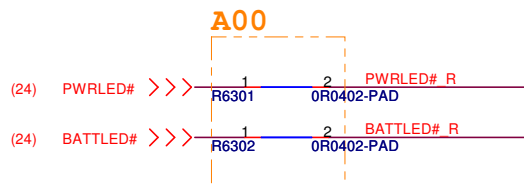
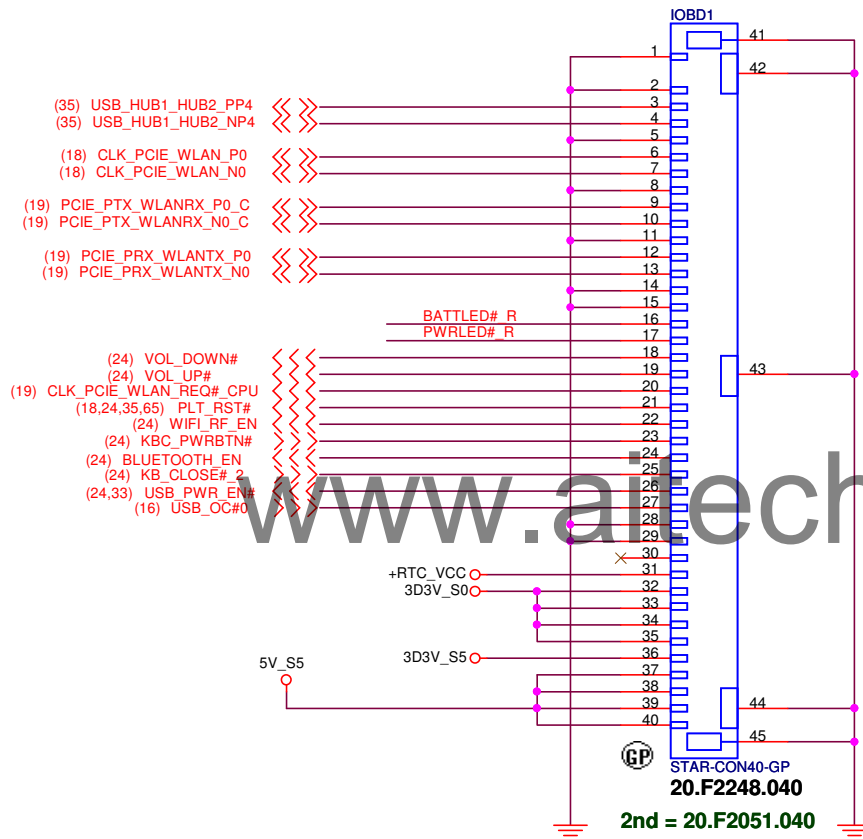
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CAP LED Control
LOW actived from KBC GPIO



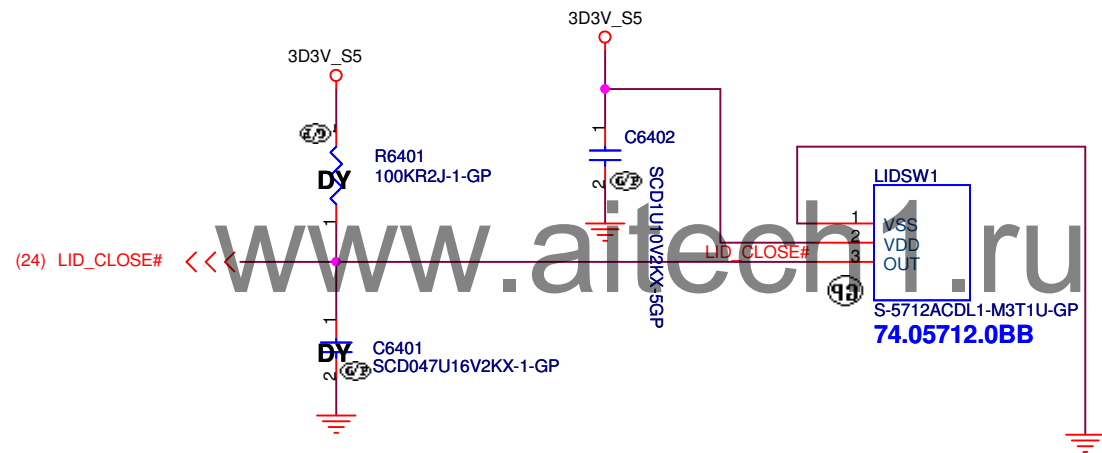


Power Pin Count : 10
GND Pin Count : 9

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Title

Hall Sensor

Size
A4

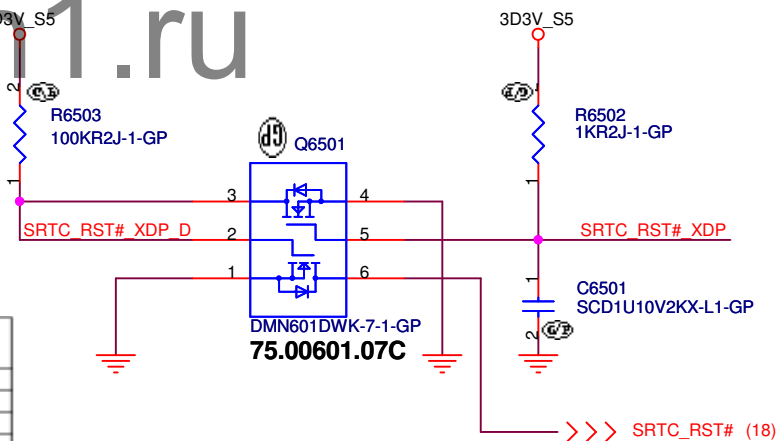
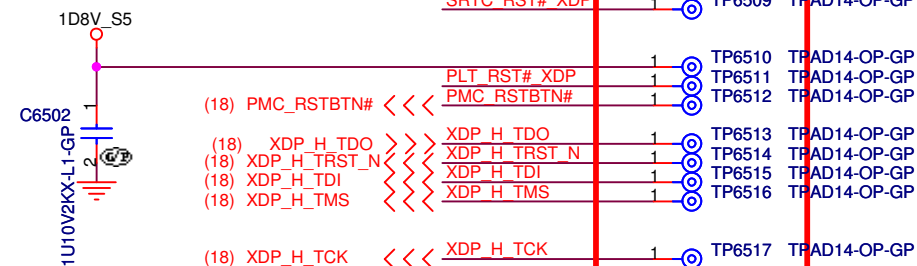
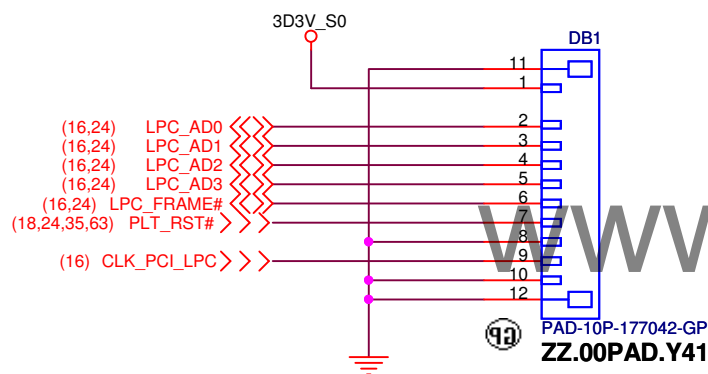
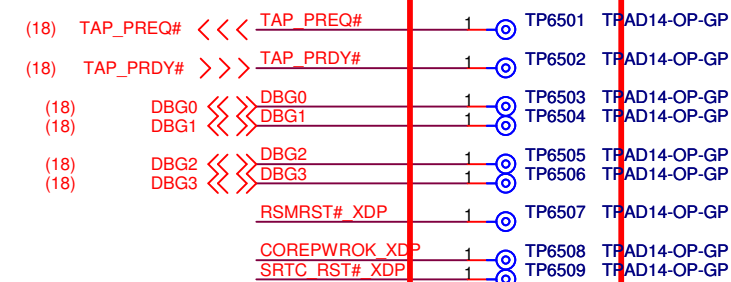
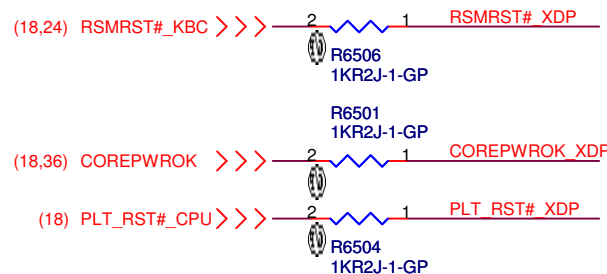
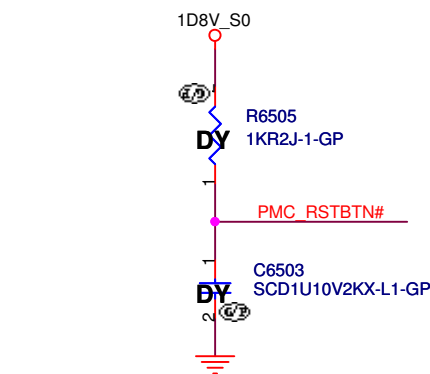
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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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Debug connector

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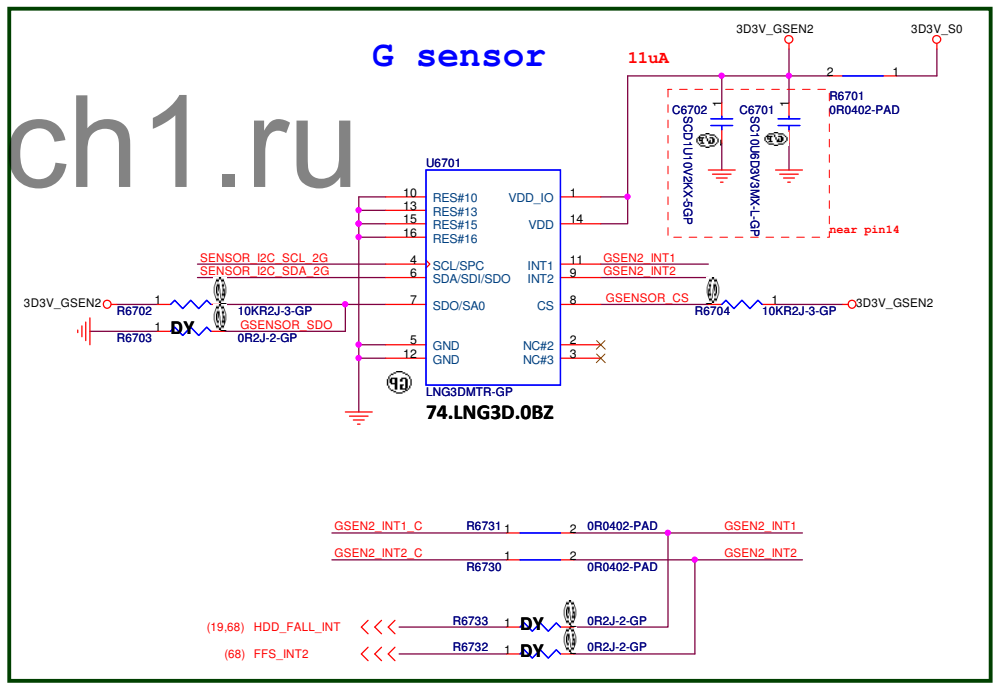
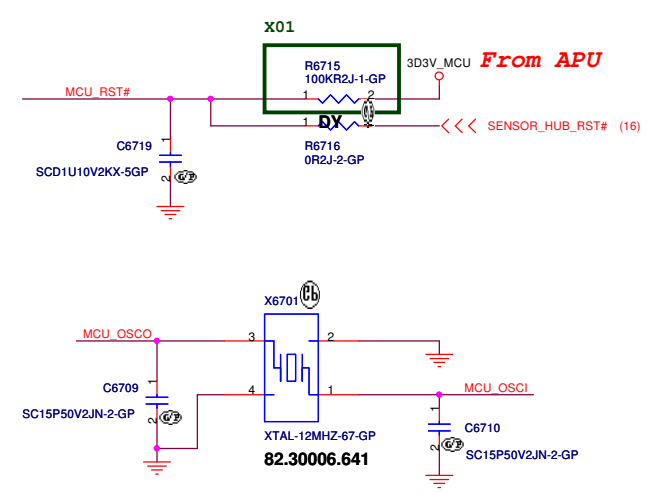
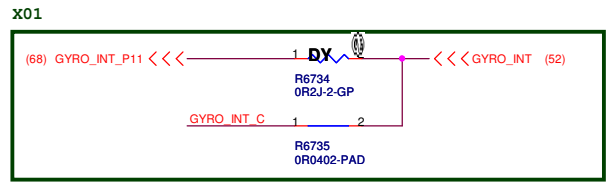
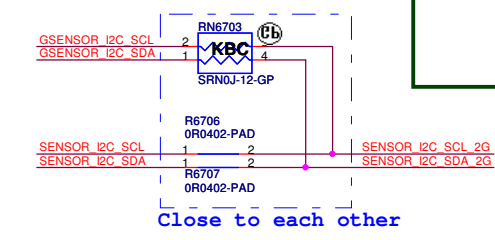
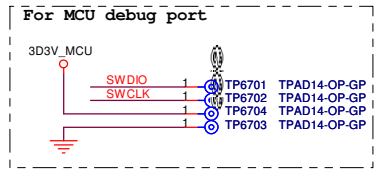
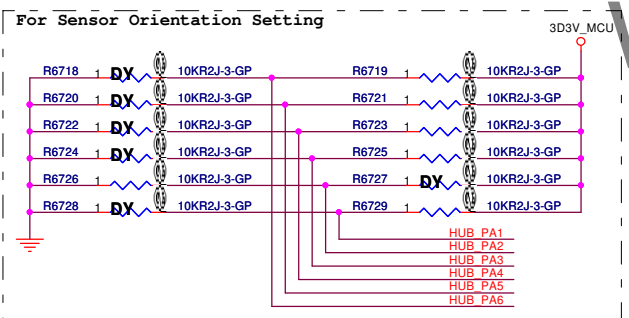
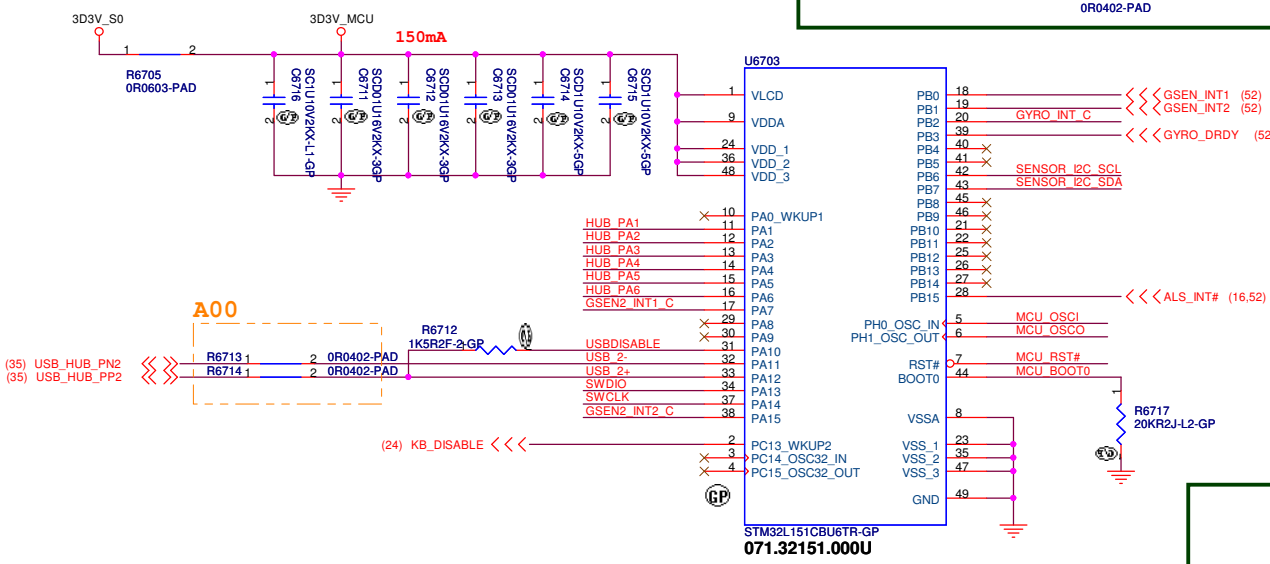
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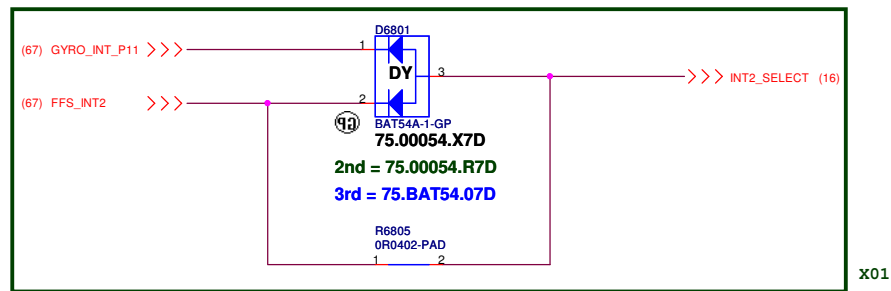
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SSID = User.Interface

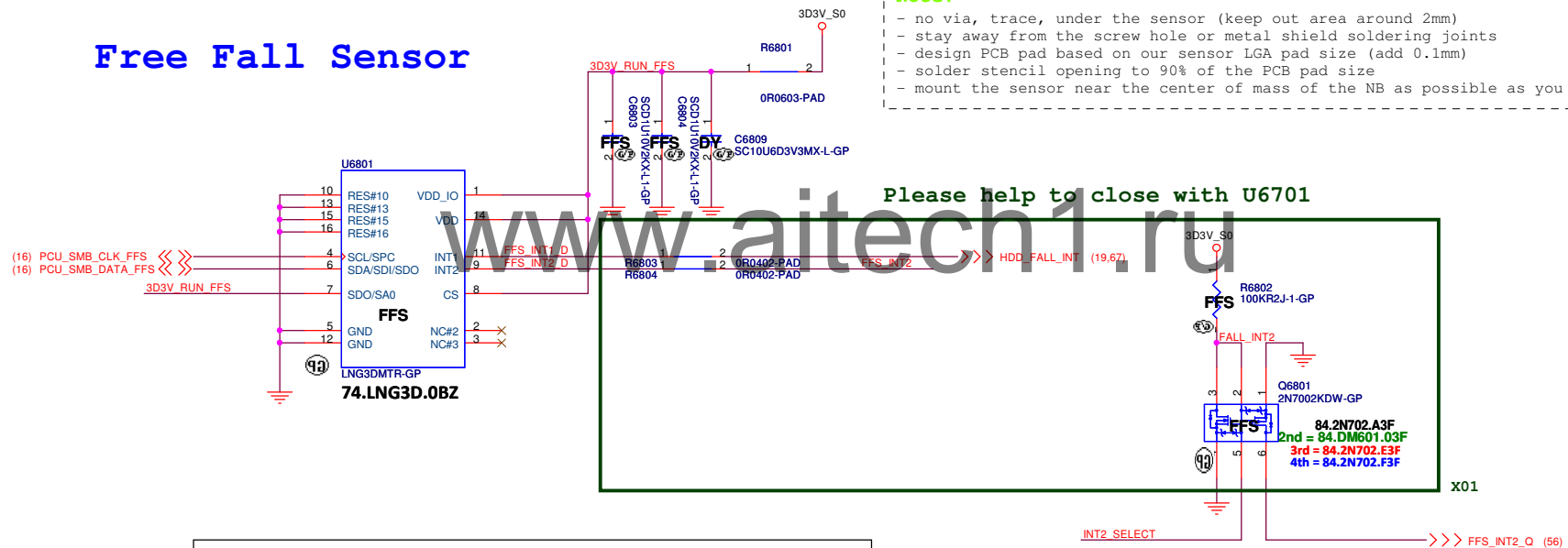
Sensor Hub



```
SSID = User.Interface
```



Free Fall Sensor



Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U6701



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Free Fall Sensor

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Title

Switchable GFX LCD(1/2)

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Title

Switchable GFX LCD(2/2)

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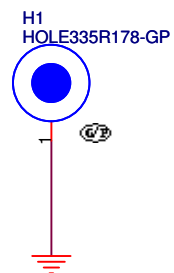
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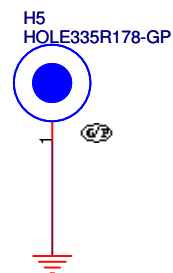
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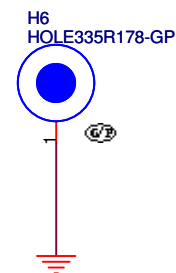
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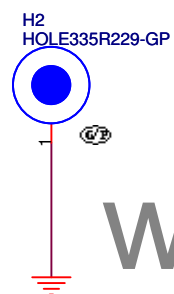
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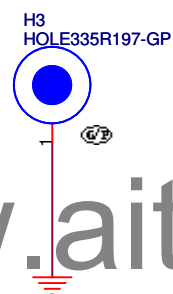
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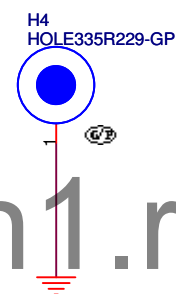
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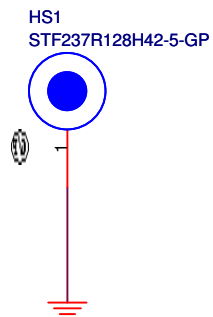


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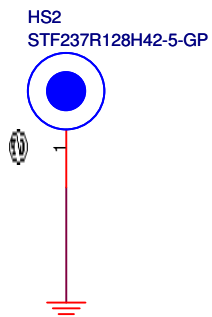
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34.4UV01.101



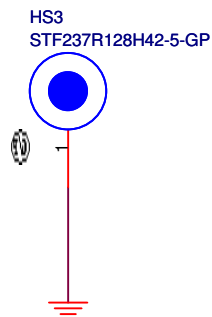
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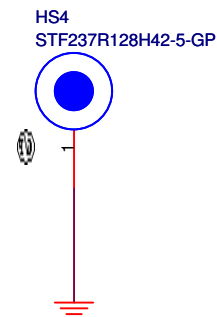
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UNUSED PARTS/EMI Capacitors

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SSID = Docking

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Title			
<i>Reserved</i>			
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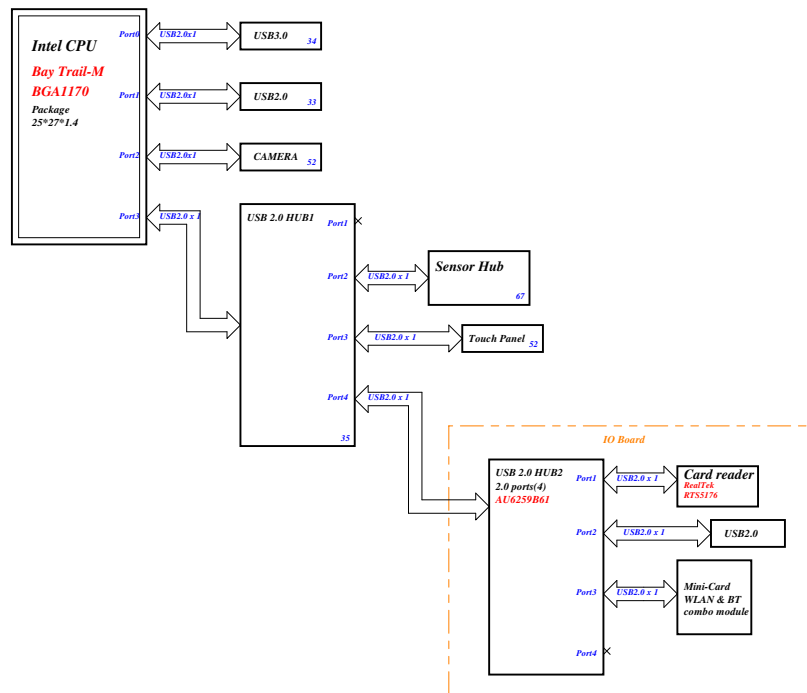
SSID = Intel LAN

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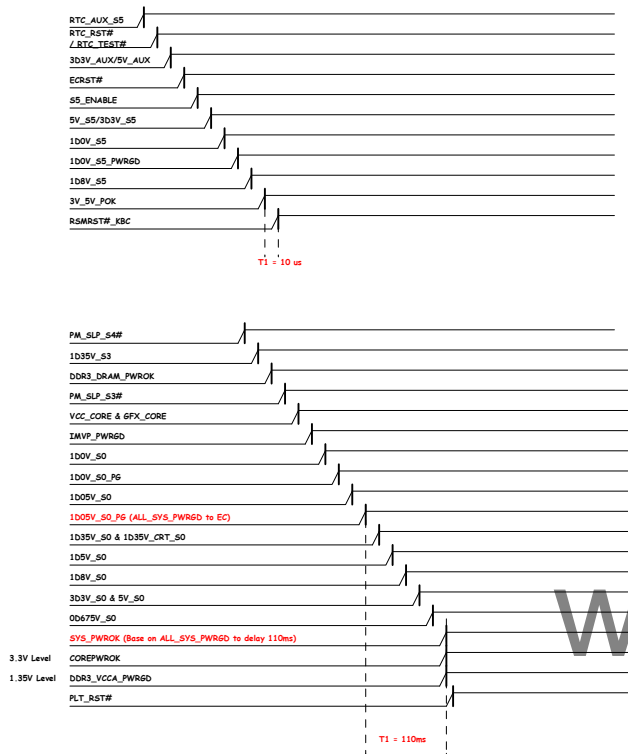
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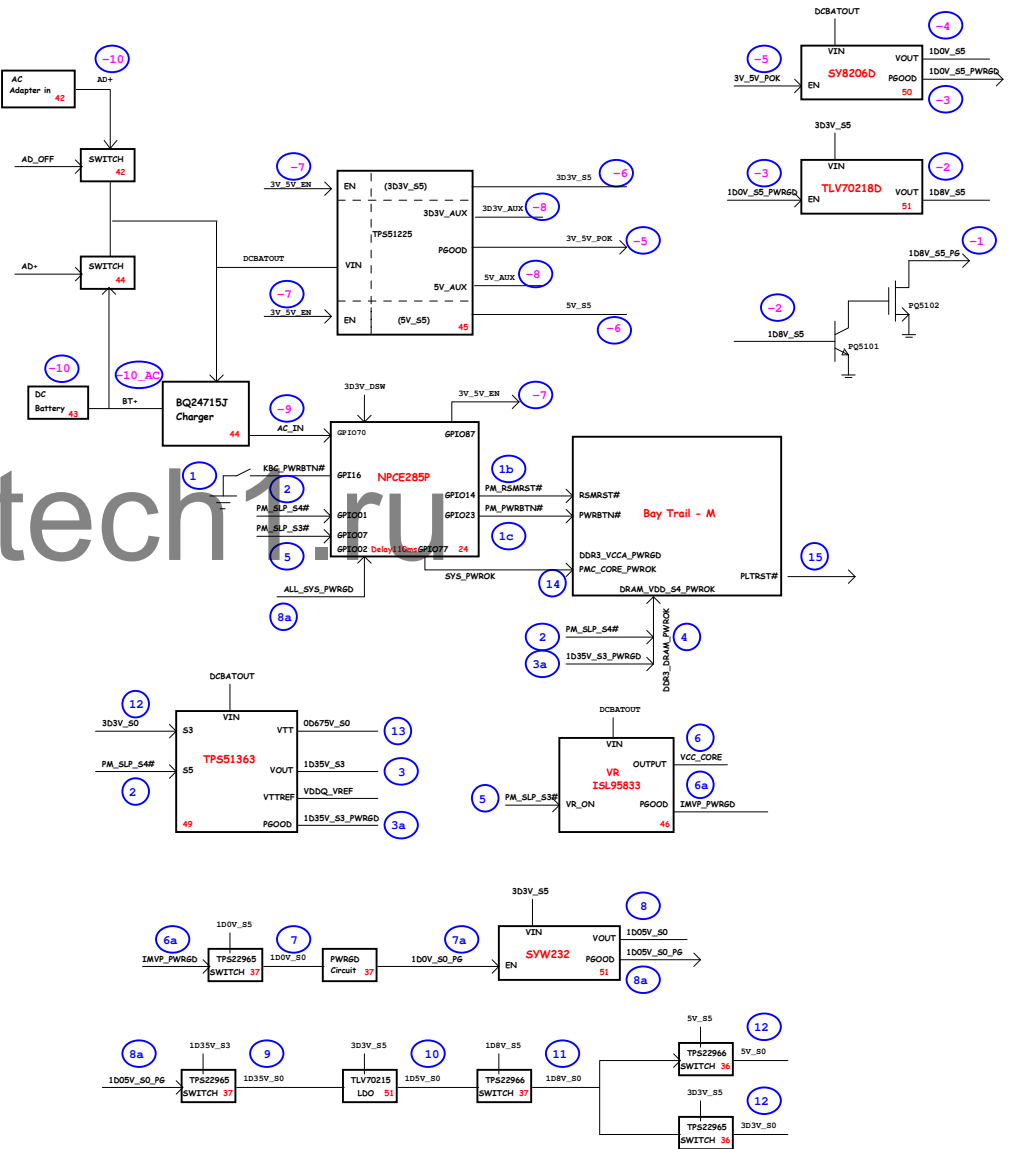
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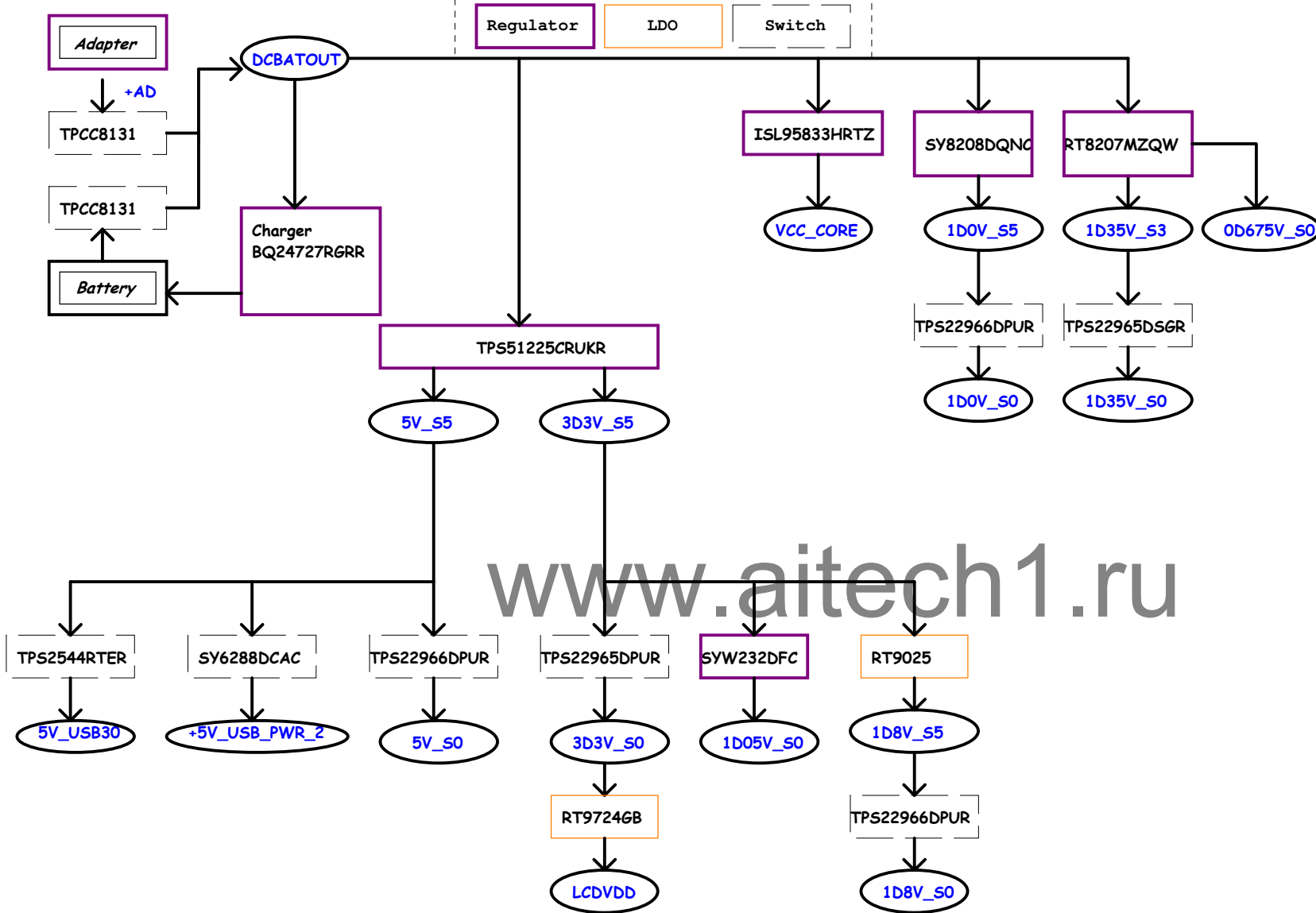
Intel-Power Up Sequence with non-S0ix



Bay Trail - M POWER UP SEQUENCE DIAGRAM



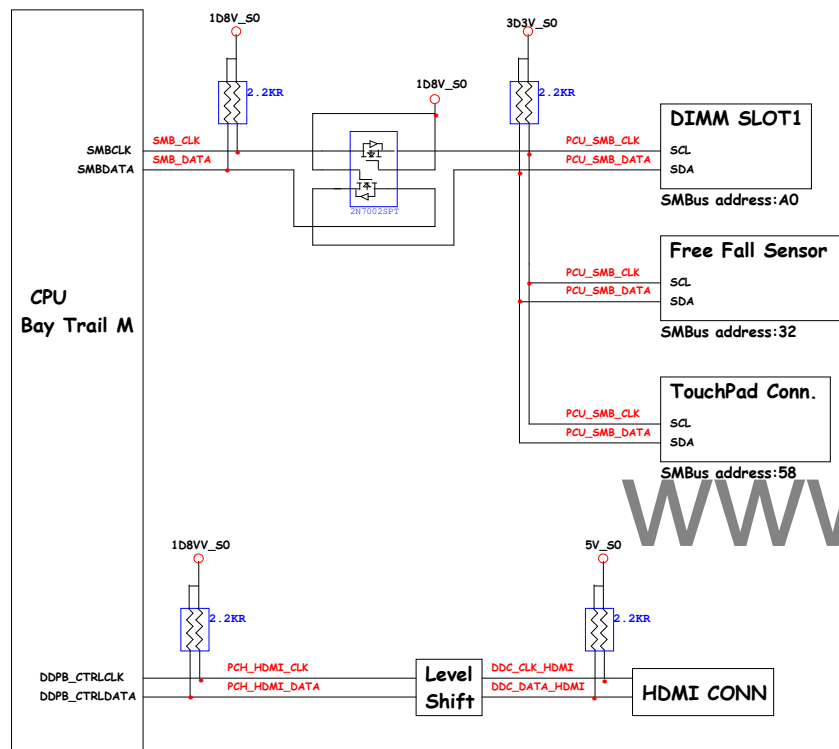
Power Shape



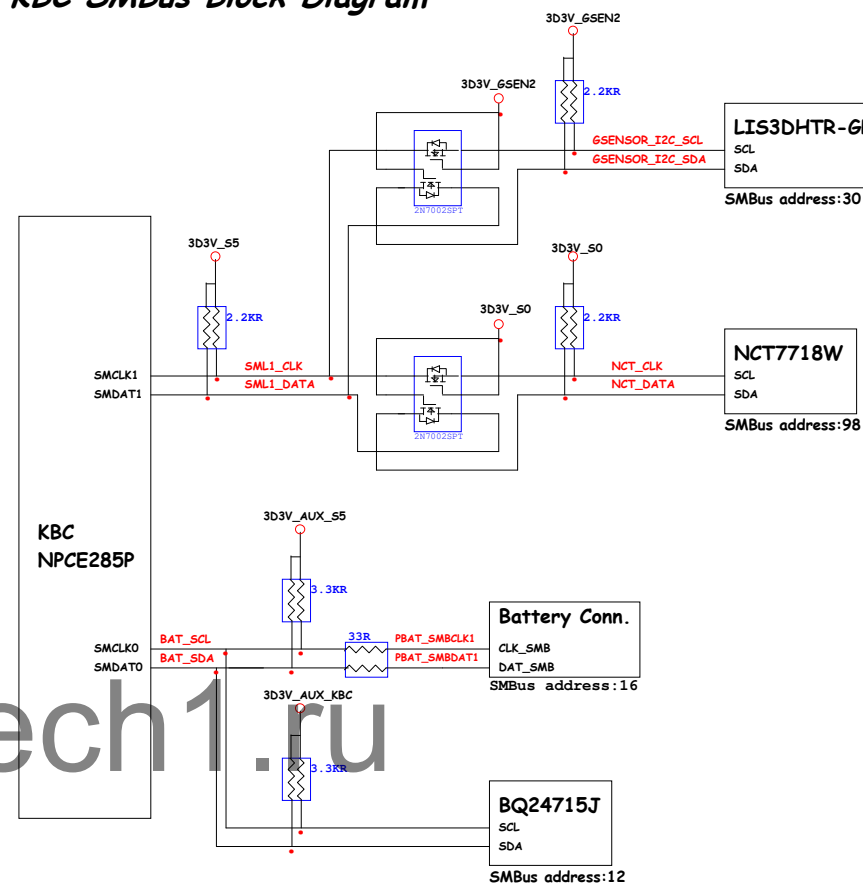
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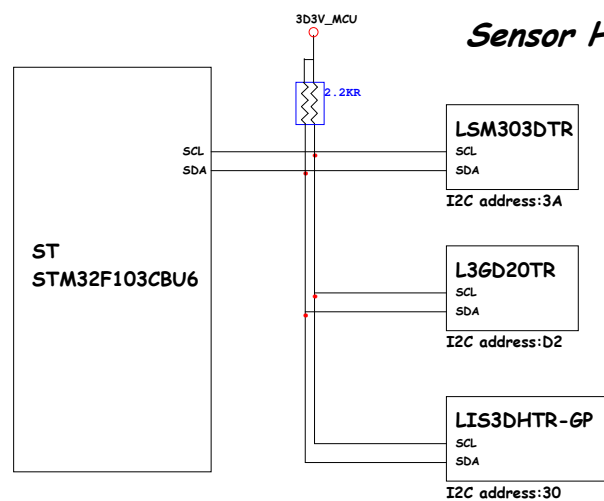
PCH SMBus Block Diagram



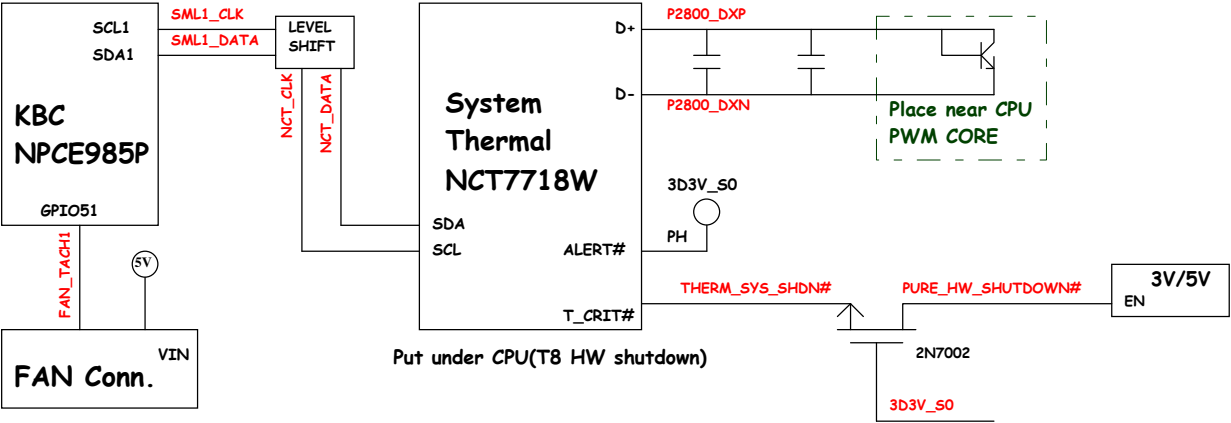
KBC SMBus Block Diagram



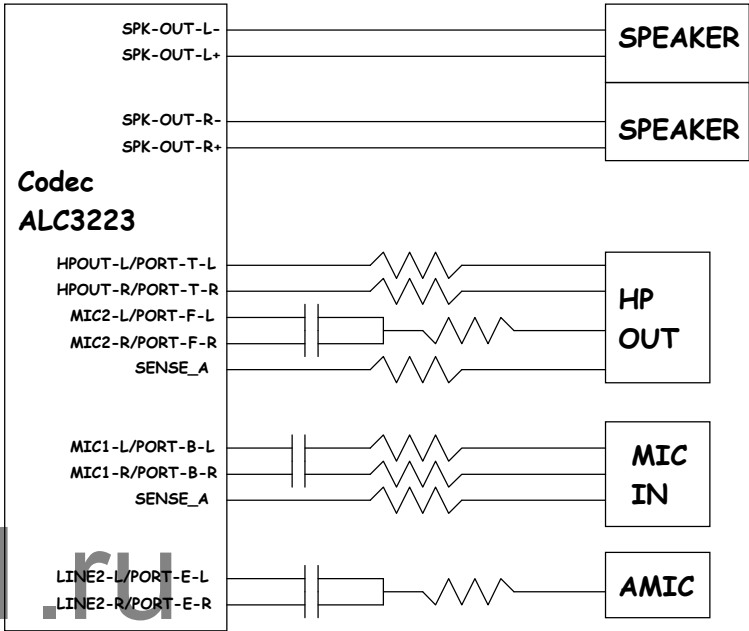
Sensor Hub I2C Block Diagram



Thermal Block Diagram



Audio Block Diagram



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